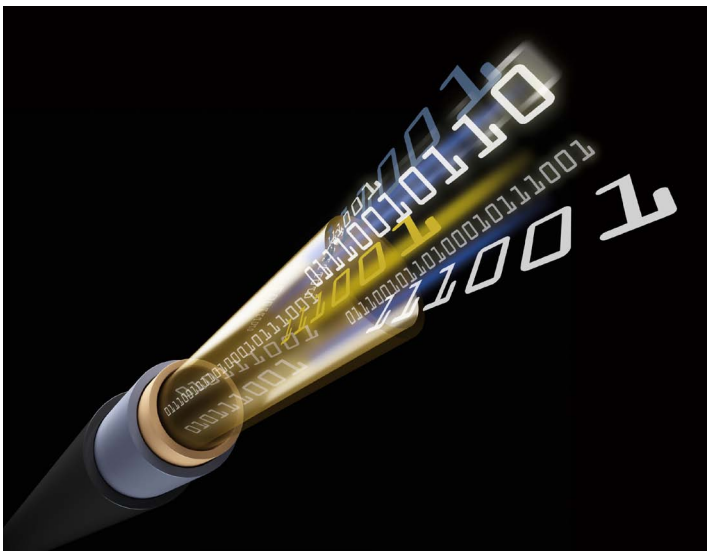
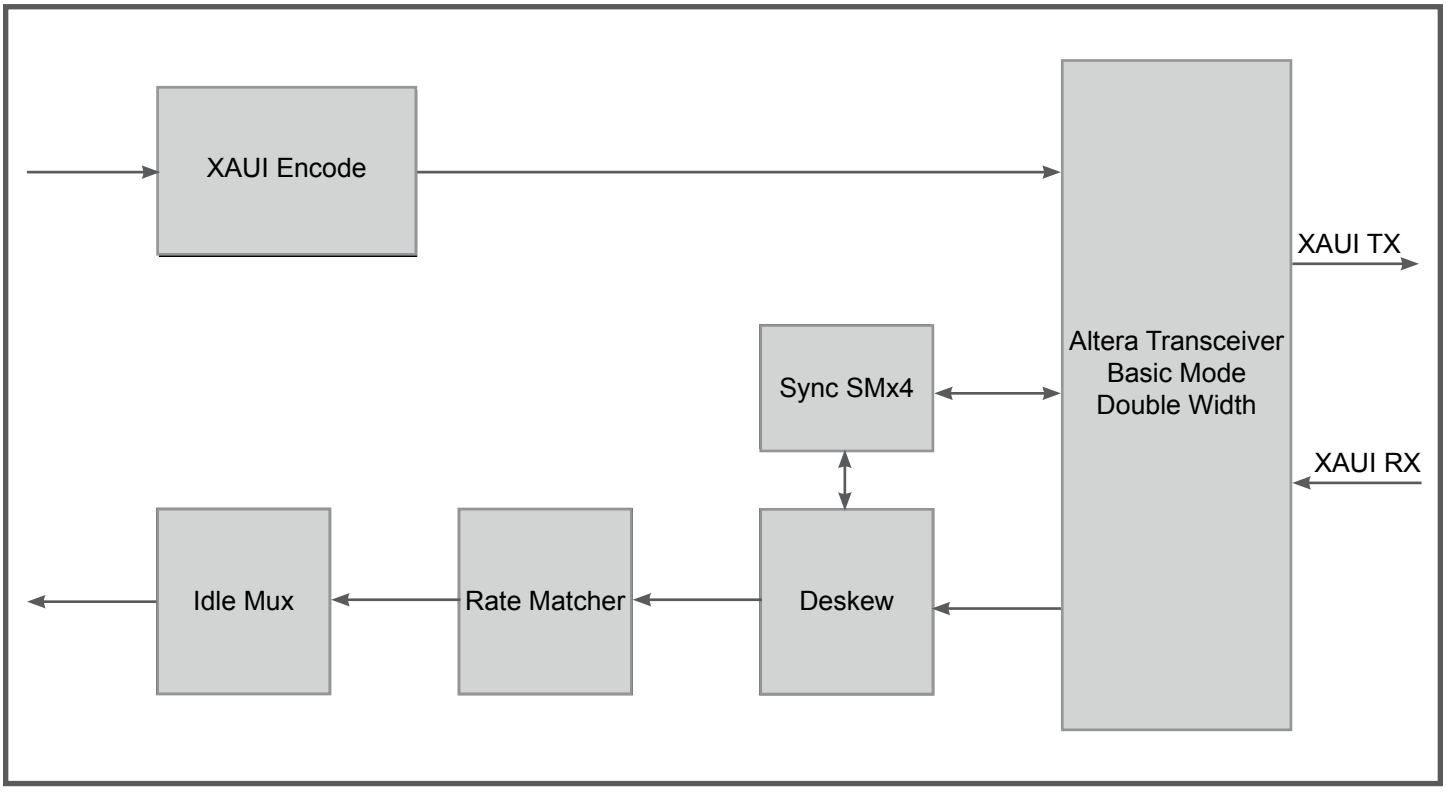
High-Speed XAUI PCS

Introduction

The Altera transceivers implement a full XAUI PCS, but only in single-width mode. In single-width mode, the serialization / de-serialization shift registers are 20-bits wide. This limits the XAUI PCS performance to 3.75 Gbps / lane.

The Macnica High Speed XAUI PCS uses the Altera transceivers are used in “basic” double-width mode. The additional modules requried to implement the XAUI PCS are implemented in the FPGA fabric. The PCS modules are implemented with a data path width of 128-bits, and are efficiently pipelined. The double-width XAUI PCS operates over the transceivers’s usable frequency range.





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Implementation Summary

CORE SPECIFICS	
Supported	Stratix IV GX and above
RESOURCES USED	
Logic Elements	3,188
Registers	3,416
RAM	5,112 bits
DSP	0
SUPPORTED DESIGN TOOLS	
Altera Tool	Quartus II 9.1 or later
SPEED GRADE	
C2 required for high-speed transceievers	

Features

- 128-bit Dta and 16-bit control MAC interface
- Deskew status, mis-alignment detection, and clock rate sync error bits in addition to transceiver status bits
- IEEE802.3 clause 48-compliant XAUI Idle En coder
- XAUI Synchronization state machine
- XAUI Lane-to-lane Deskew module
- XAUI Clock rate synchronization
- XAUI Error propgation as 1, 0xFE control character
- PMA Loopback

Customization

- If required, an Async FIFO for status bits originating in the recovered clock domain can be included
- If required, expansion from / reduction to a 64-bit data path can be included (applicable to lower speed applications)

Deliverables

- RTL source in Verilog
- ModelSim wave file (.wlf file) for transmit test with all signals logged
- ModelSim wave file (.wlf file) for receive test with all signals logged
- Full design documentation
- Example Quartus build scripts and TimeQuest constraint file