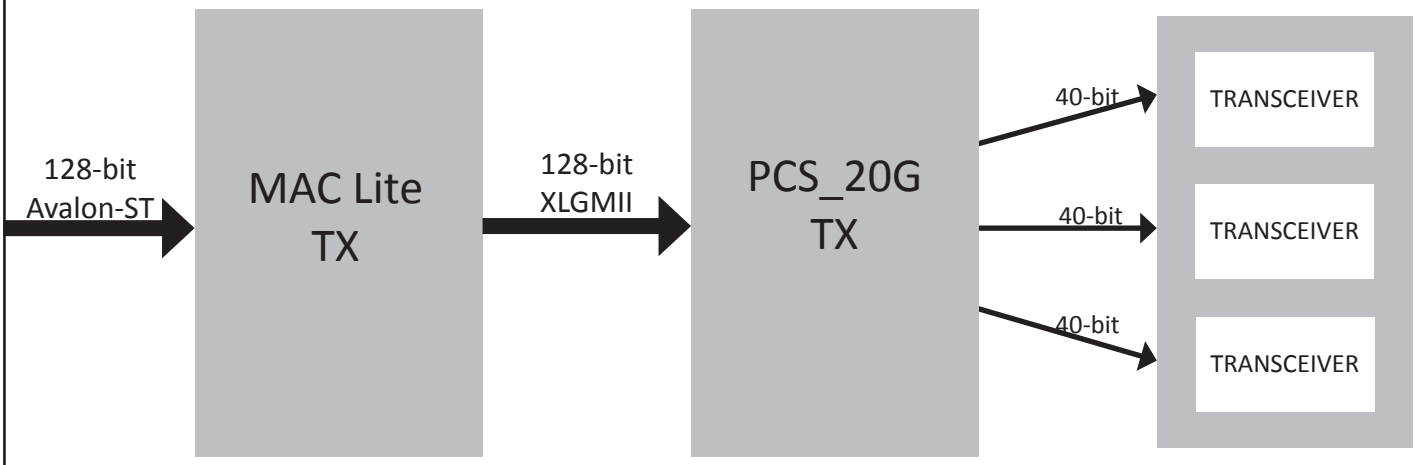
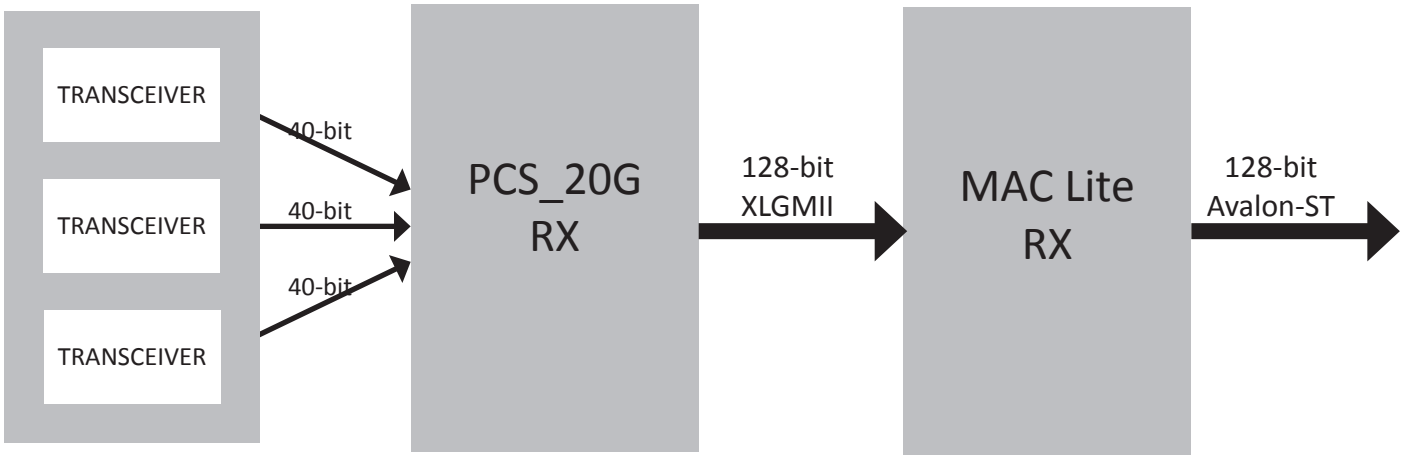
20G Chip to Chip Communication IP

The 20G Chip to Chip communication module is a small, easy to implement design allowing high-speed data transfer over 3 lanes running at 6.375Gbps. It is based on multiple Macnica 10Gbe "MACLite" Ethernet MACs and is therefore Ethernet compatible. This allows the use of external commercial switches should a more complex "crossbar" type architecture need to be implemented. The design is very resource effective using only 17k LEs and is suitable for chip to chip communications on a single PCB or over a backplane.

20G Chip to Chip Transmit Path



20G Chip to Chip Receive Path



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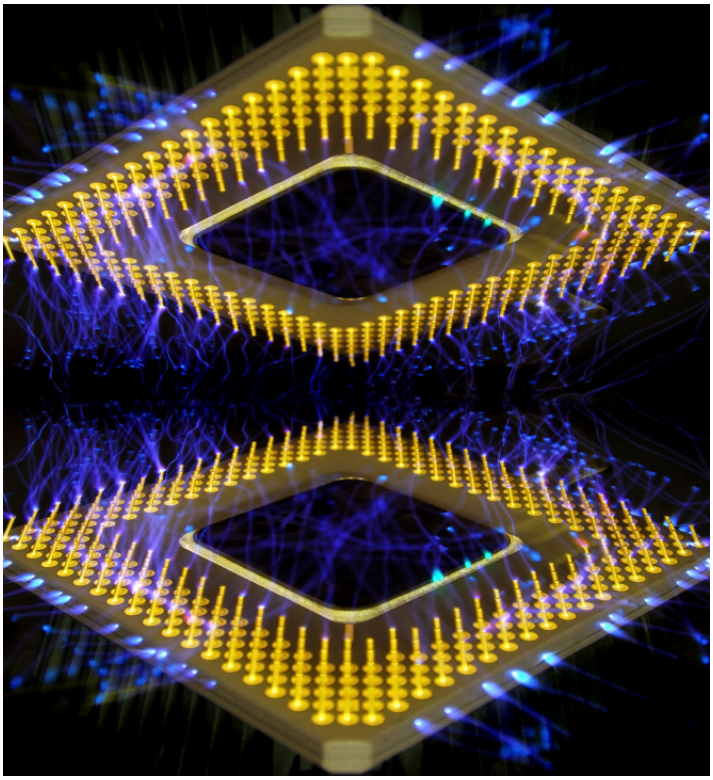
Transmit Features:

- 128-bit Avalon-ST interface, running at 17/16 times the line rate
- Cut-through packet buffer with “almost full” indication for back-pressure
- 32 or 16-bit CRC calculation and insertion
- L1 framing
  - Packing to compensate for fabric interface padding
  - SOP + 3 byte preamble insertion
  - EOP insertion
  - IPG insertion with deficit idle counter
- Interface to custom 20G PCS
- Packet and byte counters through 32-bit Avalon-MM interface

Receive Features:

- Interface to custom PCS
- Deframer and error checking with error counters
  - Fragment, oversized packet, undersized packet, and bit error counters
- 32 or 16-bit CRC checking and removal with CRC error counter
- Cut-through packet buffer with packet drop on error or when full
  - Packet drops due to buffer full are counted
  - Received good packets and bytes are counted
- All counters are read through 32-bit Avalon-MM interface



Family Supported	Arria II / Stratix IV Stratix V
Total Block Memory Bits	126k
Total Registers	14k
LEs	17k
Supported Design Tools	Quartus 12.0