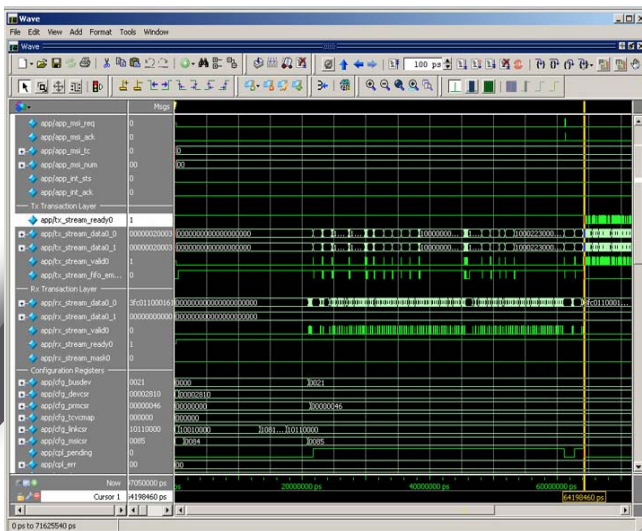


PCIe Driver Integration Tool

DrivExpress™ solves the problem of driver integration for PCIe implemented in FPGAs. PCIe is a very commonly used protocol, but implementing a custom driver-- needed for every FPGA design-- is a hard problem if all debug and testing can only be done in a FPGA HW. **DrivExpress™** provides a low cost and easy to use verification environment allowing PCIe driver and protocol issues to be tracked down and quickly resolved.

Features:

- PCIe Gen1, 2, and 3 capable (x1, x2, x4, with x16 capability)
- C++ PCIe Root Complex Model
- Allows Sophisticated PCIe System Simulations
- Python Script Driven
- Significantly Faster than Verilog Based Test Benches
- Verbose Error Reporting, Flexible Event Programming for Rapid Debug
- Essential HW / SW Integration Tool for PCIe Driver Development



```

Transcript
-----
# 00 00 01 50 00 00 01 50 00 00 01 54 00 00 01 5b
# 00 00 01 5c 00 00 00 01 54 00 00 01 5e 00 00 01 63
# 00 00 01 60 00 00 01 61 00 00 01 62 00 00 01 63
# FII Information Message from 'PCI-E Transaction Layer': Time 95668.000000: Wrote 0x80 bytes to host address 0x10001890
# 00 00 01 64 00 00 01 65 00 00 01 66 00 00 01 67
# 00 00 01 68 00 00 01 69 00 00 01 6a 00 00 01 6b
# 00 00 01 6c 00 00 01 6d 00 00 01 6e 00 00 01 6f
# 00 00 01 70 00 00 01 71 00 00 01 72 00 00 01 73
# 00 00 01 74 00 00 01 75 00 00 01 76 00 00 01 77
# 00 00 01 78 00 00 01 79 00 00 01 7a 00 00 01 7b
# 00 00 01 7c 00 00 01 7d 00 00 01 7e 00 00 01 7f
# 00 00 01 80 00 00 01 81 00 00 01 82 00 00 01 83
# FII Information Message from 'PCI-E Transaction Layer': Time 96476.000000: Wrote 0x80 bytes to host address 0x10001910
# 00 00 01 84 00 00 01 85 00 00 01 86 00 00 01 87
# 00 00 01 88 00 00 01 89 00 00 01 8a 00 00 01 8b
# 00 00 01 8c 00 00 01 8d 00 00 01 8e 00 00 01 8f
# 00 00 01 90 00 00 01 91 00 00 01 92 00 00 01 93
# 00 00 01 94 00 00 01 95 00 00 01 96 00 00 01 97
# 00 00 01 98 00 00 01 99 00 00 01 9a 00 00 01 9b
# 00 00 01 9c 00 00 01 9d 00 00 01 9e 00 00 01 9f
# 00 00 01 a0 00 00 01 a1 00 00 01 a2 00 00 01 a3
# FII Information Message from 'PCI-E Transaction Layer': Time 96764.000000: Wrote 0x30 bytes to host address 0x10001990
# 00 00 01 a4 00 00 01 a5 00 00 01 a6 00 00 01 a7
# 00 00 01 a8 00 00 01 a9 00 00 01 aa 00 00 01 ab
# 00 00 01 ac 00 00 01 ad 00 00 01 ae 00 00 01 af
# FII Information Message from 'PCI-E Transaction Layer': Time 96892.000000: Wrote 0x8 bytes to host address 0x00000000
# 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
# FII Information Message from 'Tcl Interface': Detected end of DMA Write through EPLAB Sec to last descriptor
# FII Information Message from 'Tcl Interface': No compare errors found - test passed
# FII Information Message from 'PCI-E Transaction Layer': Time 97004.000000: Wrote 0x4 bytes to host address 0xfffffff0
# 00 00 12 00
# FII Information Message from 'Command Processor': Time 97020.000000: MSI Completion Interrupt Detected - End of DMA Write
#
# FII Test Summary:
#
# 0 Errors, 0 Warnings, 194 Information Messages
# TEST COMPLETED SUCCESSFULLY!
# Break in Module cmd_p90c at ./pcie_pipe_tcl_shell.v line 34
V9M7>
    
```



DrivExpress™ PCIe *Development Flow*

