

10GbE MAC Lite

Introduction:

10GbE is a commonly used protocol both for data transmission over long stances as well as embedded communication such as high speed backplanes. A 10GbE MAC is required for both applications, however the 'fully featured' MAC designed to operate over long distances is often overly complicated and too large for short haul backplane applications.

The 10GbE MAC 'Lite' is a small, easy to use MAC for the non line-side, non-managed "local" 10GbE connections. It instantiates the Altera XAUI Hard IP, so implements the path from the FPGA fabric Avalon-ST packet interface to XAUI.







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Implementation Summary

CORE SPECIFICS	
Supported	Stratix IV GX and above
TYPICAL RESOURCES USED	
Logic Elements	1,353
Registers	1,1149
RAM	41 M9K + 32K RX / TX buffers
DSP	0
SUPPORTED DESIGN TOOLS	
Altera Tool	Quartus II 9.1 or later
SPEED GRADE	
C2 required for high-speed transceievers	

Deliverables

- Design Documentation
- Full Verilog source code
- Simulation Results
- ModelSim AE Wave file (.wmf file) with all signals logged
- 10 TX Packets of varying size from Fabric to XAUI
- 10RX Packets of varying size from XAUI to Fabric

Transmit Features:

- 64-bit Avalon-ST interface
- Parameterizable packet buffer with "almost full" indication for back pressure
- · Automatic padding for undersized packets
- CRC Calculation and Insertion
- L1 Framing
 - SOP + Preamble Insertion
 - EOP Insertion
 - IPG Insertion with Deficit Idle Counter
- Interface to Altera XAUI PCS Hard IP
- Packet and Byte counters through 32-bit Avalon-MM interface

Receive Features:

- Interface to Altera XAUI PCS Hard IP
- Deframer and error checking with error counters
 - Fragment, oversized packet, undersized packet, and bit error counters
- CRC Checking and removal with CRC Error counter
- Parameterizable packet buffer with packet drop
 on error or when full
 - · Packet drops due to buffer full are counted
 - Received good packets and bytes are counted
- All counters are read through 32-bit Avalon-MM interface