

Intellectual Property

User Guide – Rotating Video Frame Buffer

RVFB

Version 1.5

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Overview

This document describes the functionality and implementation requirements for the Rotating Video Frame Buffer. This component is intended for use with Altera's QSYS development environment as a drop-in replacement for the existing Video Frame Buffer IP in designs utilizing the Altera "VIP" or Video Image Processing Library.

This IP includes some limitations and restrictions and is not intended to be a drop-in replacement in every VIP-based application.

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Document Revision History

Revision	Date	Comments
0.01	February 20, 2013	Initial Draft
1.0	March 23, 2013	Updated to reflect new parameter options. Added memory utilization.
1.1	May 15, 2013	Added 180-degree only version for smaller footprint
1.2	June 27, 2014	Showed different top levels for 180-only version and full-featured version. Minor cleanup.
1.3	July 8th, 2014	Corrected values in control register for pitch
1.4	June 18th, 2015	Added pitch parameters for 180 version Added QSYS component figure for full version
1.5	October, 2015	Moved address multiplexing to external component for simple user customization. In the FULL rotate version added support for 10 bits per pixel

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3 Introduction and Features

3.1 Introduction

The Macnica Rotating Video Frame Buffer is a near drop-in replacement for the Altera Video Frame Buffer available in the "VIP Suite" of functions. In addition to providing a triple-buffer implementation supported frame rate conversion via dropping and repeating of video frames, it provides orthogonal (increments of 90 degrees) rotation and both vertical and horizontal reflection capabilities on a frame-by-frame basis.

3.2 Features

- QSYS-compatible
- Up to 4K x 4K resolution
- Efficient memory bandwidth utilization
- Access to diagnostic and control-related statistics:
  - Number of frames received
  - Number of frames output
  - Number of frames dropped
  - Dimensions of each frame in the buffers
  - Status of each frame (in-use, available)
- Programmable memory buffer location
- Control of orientation via Avalon Slave interface on a frame-by-frame basis
- Parameters allow reduced features for reduced logic utilization

4 References

4.1 Related Documents

Video and Image Processing User Guide, Altera Corp.

www.altera.com/literature/ug/ug_vip.pdf

Avalon Interface Specifications, Altera Corp.

www.altera.com/literature/manual/mnl_avalon_spec.pdf

5 Functional Specification

5.1 Symbol

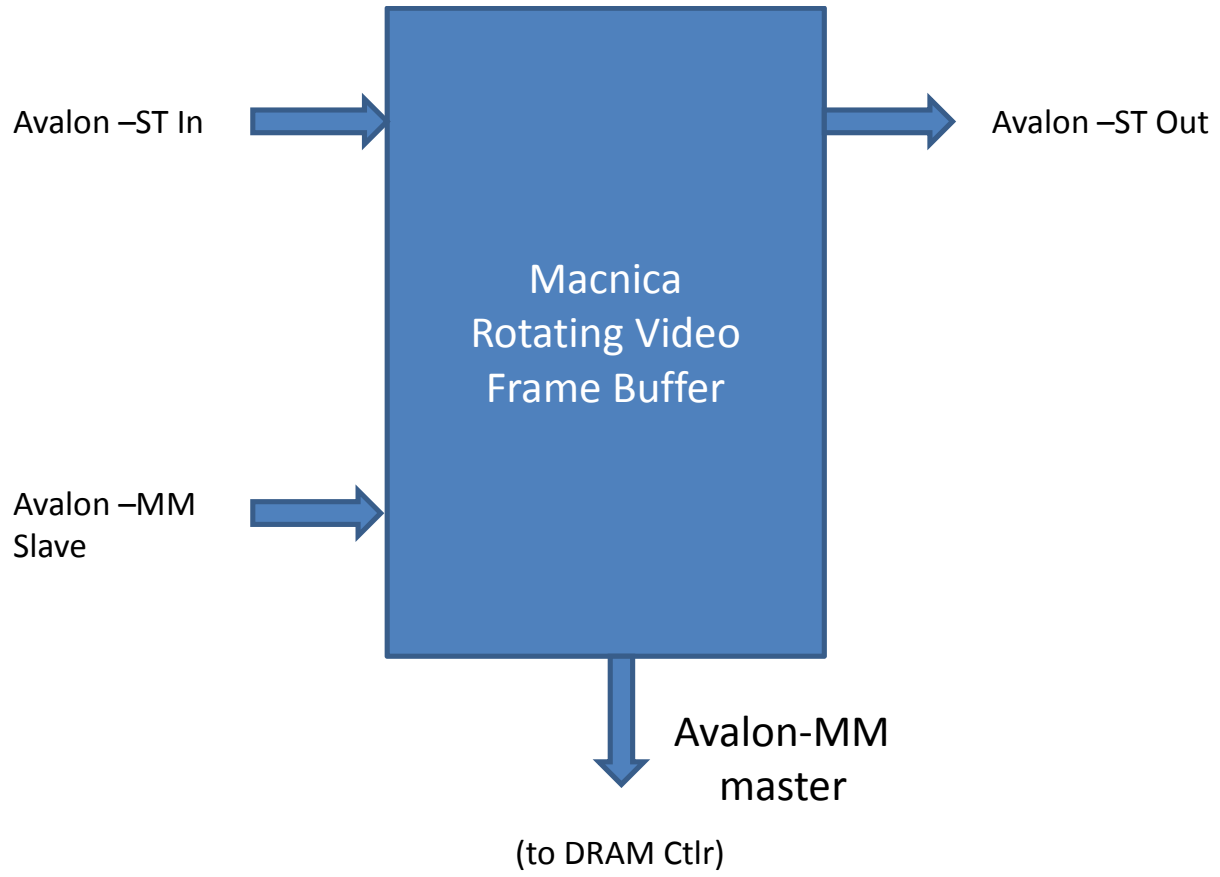

Figure 1 - Rotating Frame Buffer top-level interfaces

5.2 Interface Description

5.2.1 Control

Interface	Description	Notes
Avalon Slave	A standard Avalon Slave interface for controlling the various rotation settings and reading status	No interrupts

5.2.2 Video

Interface	Description	Notes
Avalon Streaming (source)	A standard Avalon-ST streaming video source interface	8bpp, parallel
Avalon Streaming (sink)	A standard Avalon-ST streaming video interface. Only progressive video input frames are supported.	8bpp, parallel

5.2.3 Memory

Interface	Description	Notes
Avalon Memory-Mapped master	A standard Avalon-MM Master interface that is QSYS compatible and interfaces to a fixed, 128-bit wide half-rate controller. Alternate controller interface widths are available.	8bpp, parallel

Note: Some variations of the IP have two Avalon masters – one for read accesses and one for write

5.3 Parameters

Parameter	Description	Type
BUFFER_ADDRESS	The starting buffer address in memory. Only bits [29:26] are used. Default value is zero. Buffer addresses are thus restricted to 64MB boundaries.	Std_logic_vector(31 downto 0)
ONLY_0_OR_180_DEGREES	When '1', only rotations of 0 and 180 degrees are valid. Internal FIFOs have a common clock for read and write, so the Avalon Master clock "ddr2_clk" and video path "clk" must be the same in QSYS instantiations. When '0', all rotations are available in increments of 90 degrees. Dual-clock FIFOs are used internally, so the Avalon Master and Video clocks can belong to different clock domains (only on 180-only version of the IP)	integer
SMALL_FEATURE_SET	When '1', only register zero is supported on the Avalon Slave interface. Access to frame counts, buffer status and frame dimensions (per buffer) are not available. In addition, the output frame dimensions are fixed, and incoming frame dimensions are ignored. (only on 180-only version of the IP)	Integer
FIXED_READ_WIDTH	When SMALL_FEATURE_SET is selected, output frames will be of this width regardless of the input image size. (only on 180-only version of the IP)	Std_logic_vector(15 downto 0)
FIXED_READ_HEIGHT	When SMALL_FEATURE_SET is selected, output frames will be of this height regardless of the input image size. (only on 180-only version of the IP)	Std_logic_vector(15 downto 0)
Maximum Image Width [pixels]	This parameter basically controls the address multiplexing and total size of the image buffer. Image height will be set to the same dimension	Std_logic_vector(11 downto 0) Values 512, 1024, 2048 [pixels]
BITS_PER_PIXEL_PER_ COLOR_PLANE	Full version only. Allows user to select either 8 or 10 bits per pixel color	Integer.

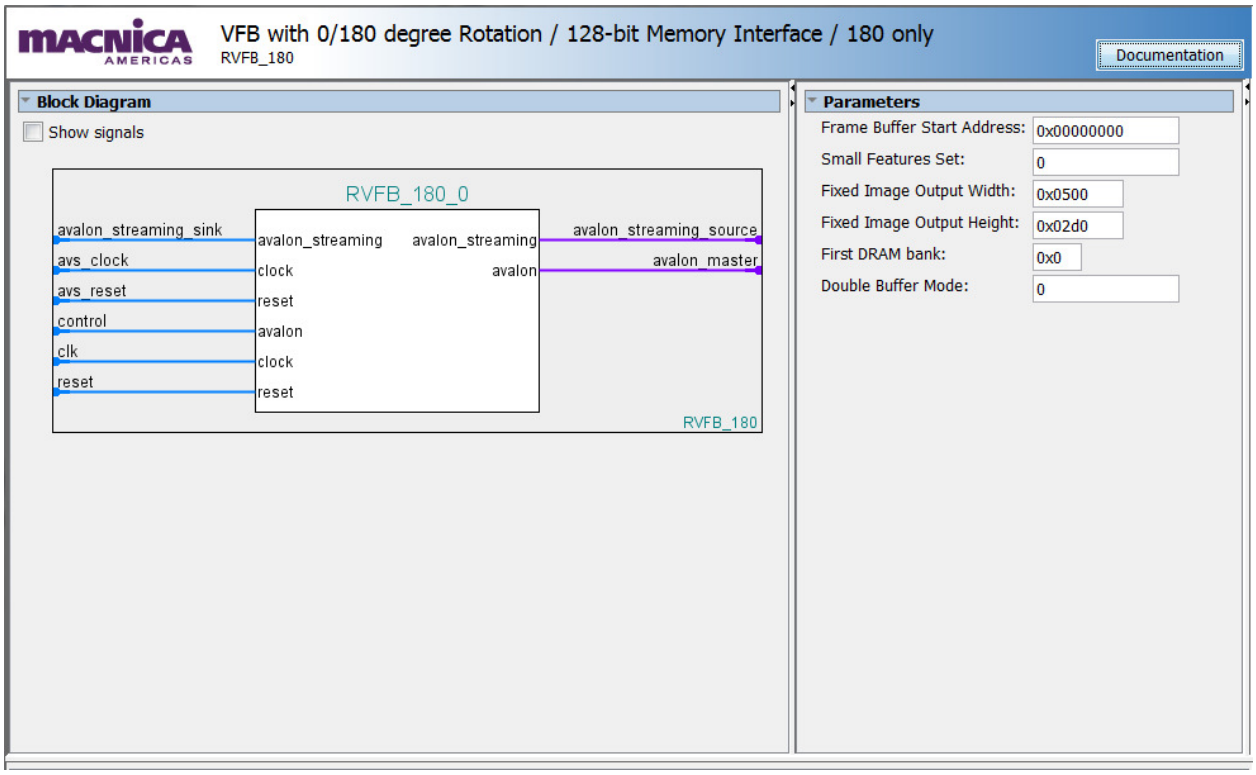

Figure 2 – QSYS Component, 0/180 only implementation, Single Master

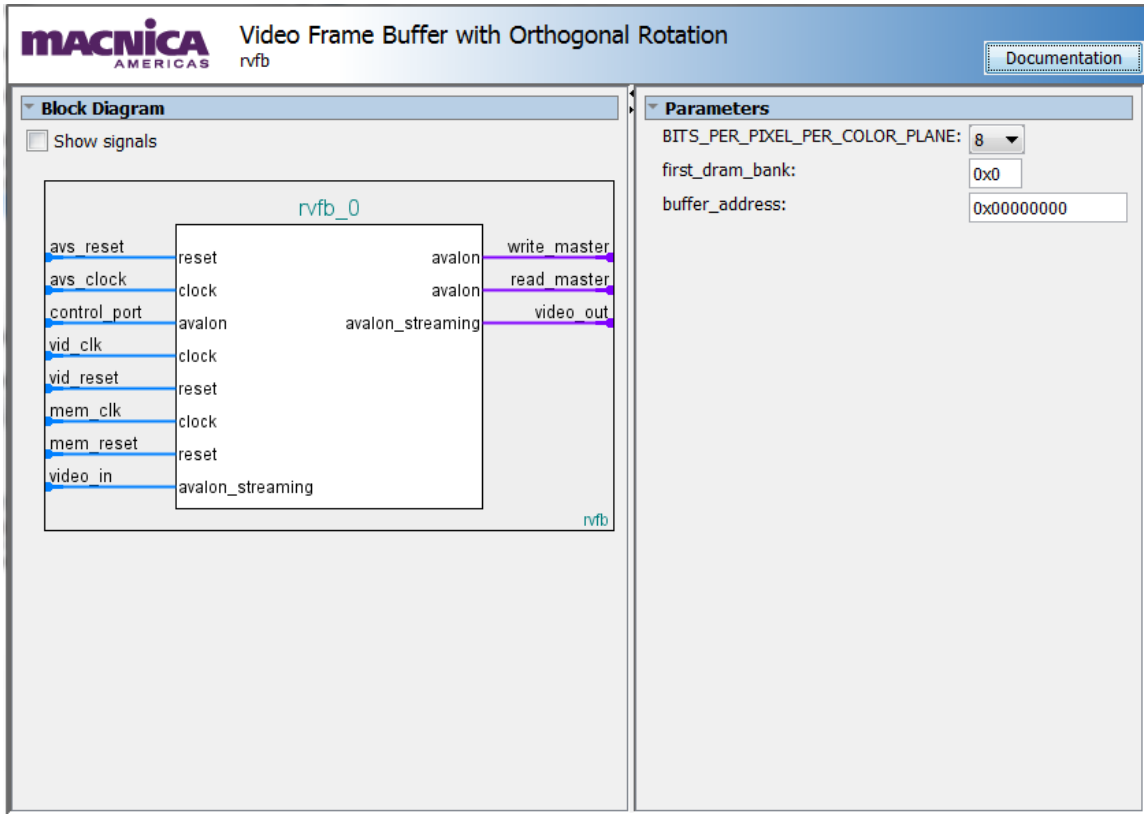

Figure 3 QSYS Component, Full Implementation, Dual Masters

5.4 Functional Description

5.4.1 Frame Input

The input portion of the R-VFB waits for a proper Control Frame from the source and will then store them incoming image into the next available buffer.

Video Frames proceeding valid Control Frames are stored regardless of the size of the input frame. No "runt frame" checking is performed. Initial frames that are preceeded only by a Start of Frame condition with no prior control packets to indicate the size of the incoming image are discarded. When multiple control frames are received prior to a valid video frame, the image dimensions and format of the last valid control frame prior to the video frame are stored and used for determining the dimensions of the output frame.

5.4.2 Frame Dropping

After receipt of a Control Frame, the input module waits for a Start of Packet for a video frame (type 0). When the Start of Frame is received, the input module checks for the availability of a free buffer to store the image. If a buffer is not available, the entire video frame is dropped and the input module waits for another Control Frame indicating the arrival of another video frame.

Upon completion of an incoming video frame, concluded with an End of Frame marker on the last pixel of input, the dimensions of the input frame are stored in an array. When this particular input frame is read for output, these stored dimensions are modified as necessary depending on the rotation settings and used in the output control packet.

When there are three frame buffers used (Double Buffer parameter is false), minimal back-pressure is applied to the source. An input FIFO will stall the incoming data briefly while data is written to memory, but this rarely occurs given sufficient memory bandwidth. In Double Buffer mode, however, the input is completely stalled when two buffers are full – i.e. one is being output, and the other is already ready with the next frame. This double buffer mode is primarily used in conjunction with a Video Frame Reader that would otherwise continue to read frames from memory that would only be dropped by the input logic.

5.4.3 Frame Output and Repeating

Once a valid frame has been stored in one of the image buffers, the output module will send out a video frame. First, it will check the values in the rotate and reflect fields of the Control Register and determine how the frame should be output. Next it will output a control frame describing the next video frame, and finally it will begin to read the frame from memory and output over the Avalon Streaming (source) interface.

Once a single frame has been output, the output module will continually output frames. It does not wait for new incoming frames. If a newer frame is available, the output module invalidates and releases the prior video frame buffer, and will output the next frame available. If a newer frame is not available, the output module will repeat the last frame that was sent.

5.4.4 Control Frames

The R-VFB does not forward any control frames in this version. Forwarding of user-defined frames or redundant Control Frames is not supported. The only Control Frames that are output from the R-VFB are those created internally and sent just prior to transmission of an output frame.

5.4.5 Storage Format

In order to simplify rotation and minimize logic utilization, pixels are stored in memory in an XRGB format whereby only 24-bits of each 32-bit word are utilized. This results in a 33% increase in memory bandwidth beyond what might be calculated based on input and output pixel rates. However, each pixel is only written once upon receipt and read once for output. No pixels are ever read from memory and discarded due to the rotation algorithms. In this sense the buffering is 100% efficient. Memory accesses are also very efficient due to bursting implementation and row/column coordination with the memory. Burst of pixels to and from the memory are continuous within a burst and there are no idle cycles inserted by the ALTMEMPHY or UNIPHY controllers.

5.4.6 Memory Usage

Memory is utilized by the frame buffer according to the largest image size supported as a power of two. For a 2K x 2K pixel image size, the memory used will be:

2048 [pixels] * 2048[lines] * 4 [bytes/pixel] * 4 [frame buffers] = 64MB

The height in memory however constitutes the upper end of the buffer addresses, and memory is used in 16-line increments with each 16 lines requiring 512KB for an input image up to 2K wide. Each 16 lines of the input image requires 16 [lines] * Width rounded up to 2^n boundary [pixels] * 4 [frame buffers] * 4 [bytes per pixel]. As the BUFFER_ADDRESS contributes only to addresses [29:26], BUFFER_ADDRESS values are restricted to 64MB boundaries

In the 180-only version, the address multiplexing can be completely controlled by the user via a clear-text module address_mux.vhd provided. Ideally, in some systems, it can be most effective to implement Chip_Select/Row/Bank/Column addressing, and the input buffer bits (3) are aligned to the BANK bits so that the current input frame and output frame are always in separate memory banks and will thus never collide which would require rows to be closed and opened repeatedly. Every system is different – but the flexibility provided also allows for the user to minimize the memory footprint but not using X/Y address indices beyond the maximum dimension.

6 Control and Status Registers

6.1 Registers

Register	Description	Notes
Control Register (address 0)	This is the standard VIP control register. As usual, bit '0' is the "Go" bit that enables the module. Additional bits are: [2:1] Rotation desired in increments of 90 degrees: "00" = no rotation "01" = 90-degree rotation "00" = 180-degree rotation "00" = 270-degree rotation [3] Horizontal reflection. When '1', rotation is performed as specified by the rotation selected in bits [2:1], and then a horizontal reflection is applied [4] Vertical reflection. When '1', rotation is performed as specified by the rotation selected in bits [2:1], and then a vertical reflection is applied [6:5] image Pitch. This value controls the amount of memory allocated per line of the image. "00" = 1K pixels per line "01" = 2K pixels per line "10" = 4K pixels per line "11" = 8K pixels per line	No interrupts
Buffer Start (address 1)	Obsolete. Buffer addresses are set via Parameter in QSYS instantiation.	
Frames (address 2)	This register shows the number of frames that have been received by the VFB and how many frames have been output by the VFB. [15:0] Frames Output [31:16] Frames Input	
Status (Address 3)	This register shows various status regarding the frame buffers [15:0] Frames Dropped. This is the number of frames that we discarded prior to storage in any buffers due to lack of available buffers. [18:16] Frame Valid. This field shows the status of the three buffers used for video frame storage. A '1' indicates that a frame is present in the buffer. One bit indicates the status of each of the buffers [2:0] in that order. [24] Dout_Ready. This bit reflects that state of the dout_ready signal on the output interface [26:25] This value indicates the frame that is currently in use for storage the next, or currently incoming, video frame. Only values 0, 1, and 2 are valid as there are only three frames. [28:27] This value indicates the frame that is currently outputting a frame	

	[29] This value shows that the output stage is busy outputting a line. It is used mainly for debug purposes.	
Dimensions(0) (address 4)	This register shows the dimensions of the current frame in buffer zero. The format is: [31:16] Image Width [15:0] Image Height	Values indicated dimensions on input of frame
Dimensions(1) (address 5)	Dimensions for frame buffer one	
Dimensions(2) (address 6)	Dimensions for frame buffer two	

7 Specifications

7.1 Image Size

The Rotating Video Frame Buffer supports image dimensions of up to 4K x 4K. Larger dimensions can be supported and are customized for customer applications.

7.2 Performance

The video frame buffer meets timing for 1080p operation at a video rate of 148.5 MHz. Fmax exceeds 151 Mhz in a typical implementation on Cyclone V.

7.3 Memory Interface

The Avalon Memory-Mapped interface connects the R_VFB to a DDR2/3 SDRAM controller based on ALTMEMPHY or UNIPHY. The width of the local interface is 128 bits, typically with a "half-rate" implementation. Support for other local interface widths is possible – contact Macnica Design Services for details regarding customization.

8 Resource Utilization

Target Device Family	Variation	Memory	ALM
Cyclone V	0/180 degrees only	12 M10K 73728 bits	1386 [A-B+C]
Cyclone V	0/180 degrees only, SMALL_FEATURE_SET	12 M10K 73728 bits	700 [A-B+C]
Cyclone V	Full rotation support Half-rate DDR controller	90 M10K 811008	1241 [A-B+C]
Cyclone III	Full rotation support Full-rate DDR controller	51 M9K 411648 bits	1267 [A-B+C]