Nisshinbo Micro Devices Inc.

PRELIMINARY SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

NB7130ZA Series

1-cell Li-ion Battery Protection IC for Low-side FETs

FEATURES

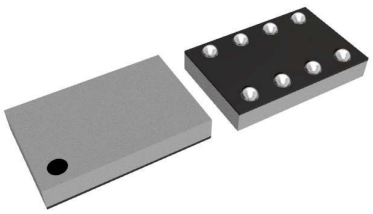
- Supply Current
  Normal mode: Typ. 3.00 µA / Max. 6.00 µA
  Standby mode: Max. 0.04 µA
- Detector Selectable Range and Accuracy
  Overcharge Detection Voltage (V_{DET1}):
  4.3 V to 4.8 V, ±6.5 mV
  Over-discharge Detection Voltage (V_{DET2}):
  2.0 V to 3.0 V, ±17 mV
  Discharge Overcurrent Detection Voltage (V_{DET3}):
  0.0060 V to 0.0500 V, ±0.75 mV
  Charge Overcurrent Detection Voltage (V_{DET4}):
  –0.0060 V to –0.0500 V, ±0.75 mV
  Short Circuit Detection Voltage (V_{SHORT}):
  0.0200 V ≤ V_{SHORT} ≤ 0.0800 V, ±1.00 mV
  0.0800 V < V_{SHORT} ≤ 0.1250 V, ±2.00 mV
- 0 V Battery Charging selectable: Permission / Inhibition
  0 V Battery Charging Inhibition Voltage (V_{NOCHG}):
  1.200 V to 2.000 V, ±20.0 mV
- Overtemperature Detection temperature (T_{DET}):
  40°C to 85°C, ±2.0°C
- Over-discharge Release Type selectable:
  Latch / Latch with Hysteresis
- Discharge Overcurrent Release Type selectable:
  Auto Release /Latch

APPLICATIONS

- Hearable / Wearable devices,
- Smart Phone,
- Handheld Data Terminals

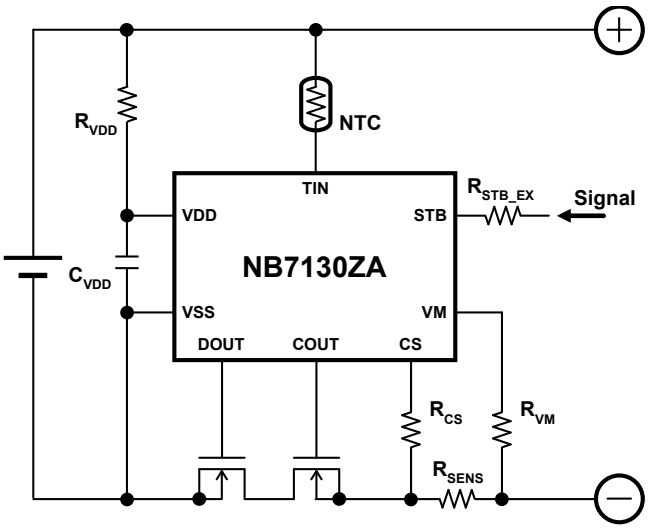
GENERAL DESCRIPTION

The NB7130ZA is one-cell Li-ion / Li-polymer rechargeable battery protection IC features high-accuracy overcharge, over-discharge, overcurrent, and a short circuit current protector.
TheNB7130ZA further includes temperature protections and forced standby mode. It's possible to detect the temperature by connecting a thermistor.
The COUT and DOUT outputs (CMOS output) are normally High.
When the NB7130ZA detects any abnormal condition to stop charging or discharging, either the COUT or the DOUT output becomes Low. Only in the abnormal temperature condition, both the COUT and DOUT outputs may become Low.



WLCSP-8-ZA1
1.65 x 0.97 x 0.40 *1 [mm]
*1 Maximum thickness including balls

TYPICAL APPLICATION CIRCUIT



PRODUCT NAME INFORMATION

NB7130	ZA	***	*	*	E2	S
	aa	bbb	c	d	ee	f

Description of configuration

Composition	Item	Description
aa	Package	Indicates the package code.
bbb	Specific Option	Indicates a three-digit number code that combined set voltages. Refer to the table of set voltages for details.
c		Indicates a delay time code. Refer to the table of delay times for details.
d		Indicates a function code. Refer to the table of functions for details.
ee	Packing	Indicates the taping code of the package. Refer to Packing Specification in the appendix Package Information for details.
f	Grade	Indicates the quality grade. S: Standard Refer to the table of grade for details.

Table of set voltage and temperature (bbb)

Symbol	V_{DET1}	V_{DET2} *1	V_{DET3} *1	V_{REL3}	V_{DET4}	V_{SHORT1} *1	V_{NOCHG} *1	$T_{DET1/2}$	$T_{REL1/2}$ *2	NTC[kΩ]
Range [V] / [°C] (Step)	4.3 to 4.8 (0.001)	2.0 to 3.0 (0.001)	0.0060 to 0.0500 (0.0001)	V_{DD} x 0.13 / 0.20 / 0.04 / 0.00	–0.0060 to –0.0500 (0.0001)	0.0200 to 0.1250 (0.0001)	1.200 to 2.000 (0.001)	40°C to 85°C (5)	$T_{DET1/2}$ – [5 to 10] (5)	100 / 470

*1 $V_{DET2} - V_{NOCHG} \geq 200$ mV,
$V_{SHORT1} - V_{DET3} \geq 14$ mV

*2 Each set value of $T_{REL1/2}$ can be set to 5°C to 10°C (in steps of 5°C) lower than $T_{DET1/2}$.

Table of delay times (c)

Symbol	t_{VDET1}	t_{VREL1}	t_{VDET2}	t_{VREL2}	t_{VDET3}	t_{VREL3}	t_{VDET4}	t_{VREL4}	$t_{VSHORT1}$	t_{TDET}	t_{TON}	t_{TOFF}	$t_{VSTBDET}$ *1	$t_{VSTBREL}$ *1
Time [ms]	256 / 1024 / 4096	2.1	16 / 32 / 128 / 256	1.1	16 / 32 / 128 / 512 / 1024 / 2048	1.1	8 / 16 / 32 / 512	1.1	0.28 / 0.53 / 1.1 / 2.1	512 / 1024 / 4096	8	128 / 512	1.1 / 16	16 / 128
B	4096	2.1	256	1.1	512	1.1	512	1.1	1.1	1024	8	512	-	-
C	4096	2.1	16	1.1	16	1.1	512	1.1	1.1	1024	8	512	-	-
D	1024	2.1	32	1.1	1024	1.1	32	1.1	0.28	512	8	128	1.1	128

*1 When forced standby is available, $t_{VSTBDET}$ and $t_{VSTBREL}$ are enabled.

Table of functions (d)

Function	Release Option			0 V Battery Charging	Temperature Protection	Forced Standby	Forced Standby Option	
	Overcharge	Over-discharge	Discharge Overcurrent				STB Pin	V_{STBREL} *1
Type / Condition	Latch	Latch / Latch with Hysteresis	Auto Release / Latch	Permission / Inhibition	High Temp.	Enabled / Disabled	Active-high / low	V_{REL3} / V_{REL4}
G	Latch	Latch with Hysteresis	Latch	Inhibition	High Temp.	Disabled	-	-
J	Latch	Latch	Auto Release	Inhibition	High Temp.	Enabled	Active-high	V_{REL3}

*1 When forced standby is available, V_{STBREL} is specified with a value equal to V_{REL3} or V_{REL4}.

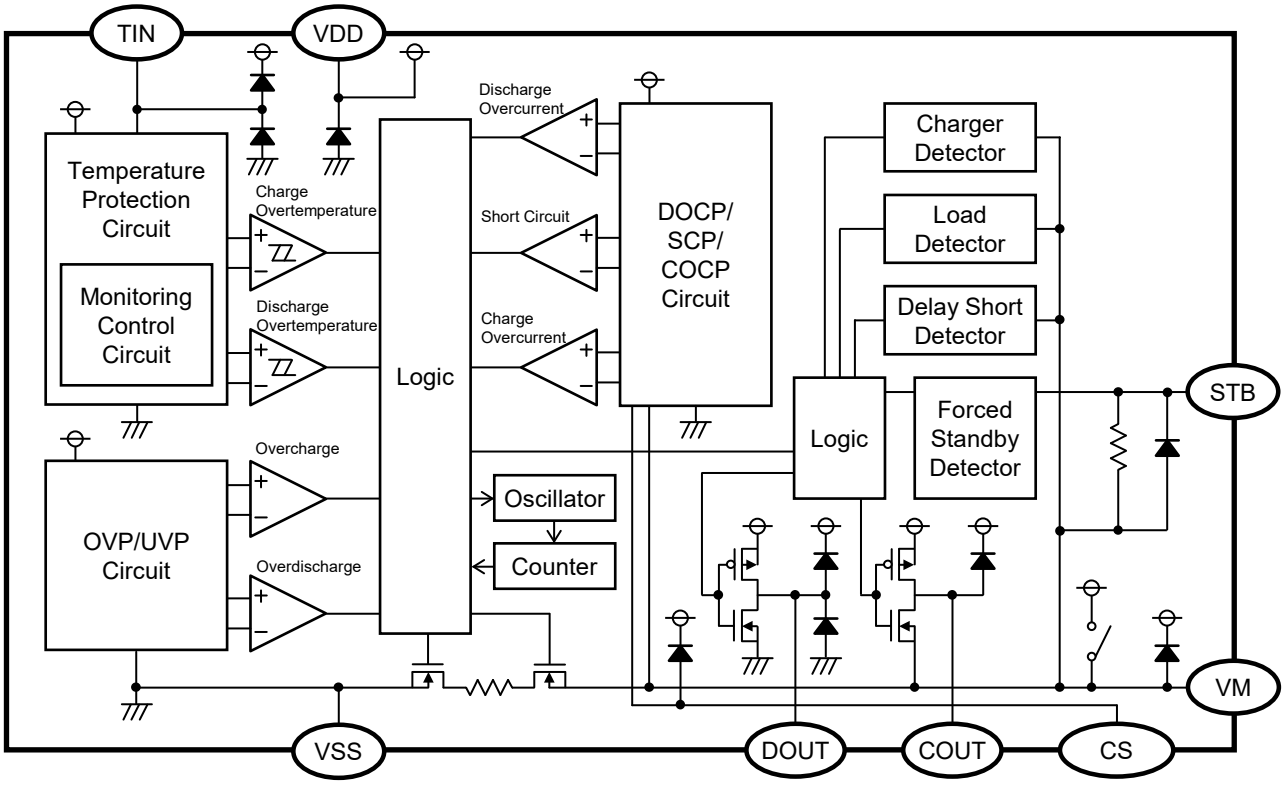
Table of grade (f)

	Applications	Operating Temperature Range	Test Temperature
S	General−purpose and Consumer application	-40°C to 105°C	25°C

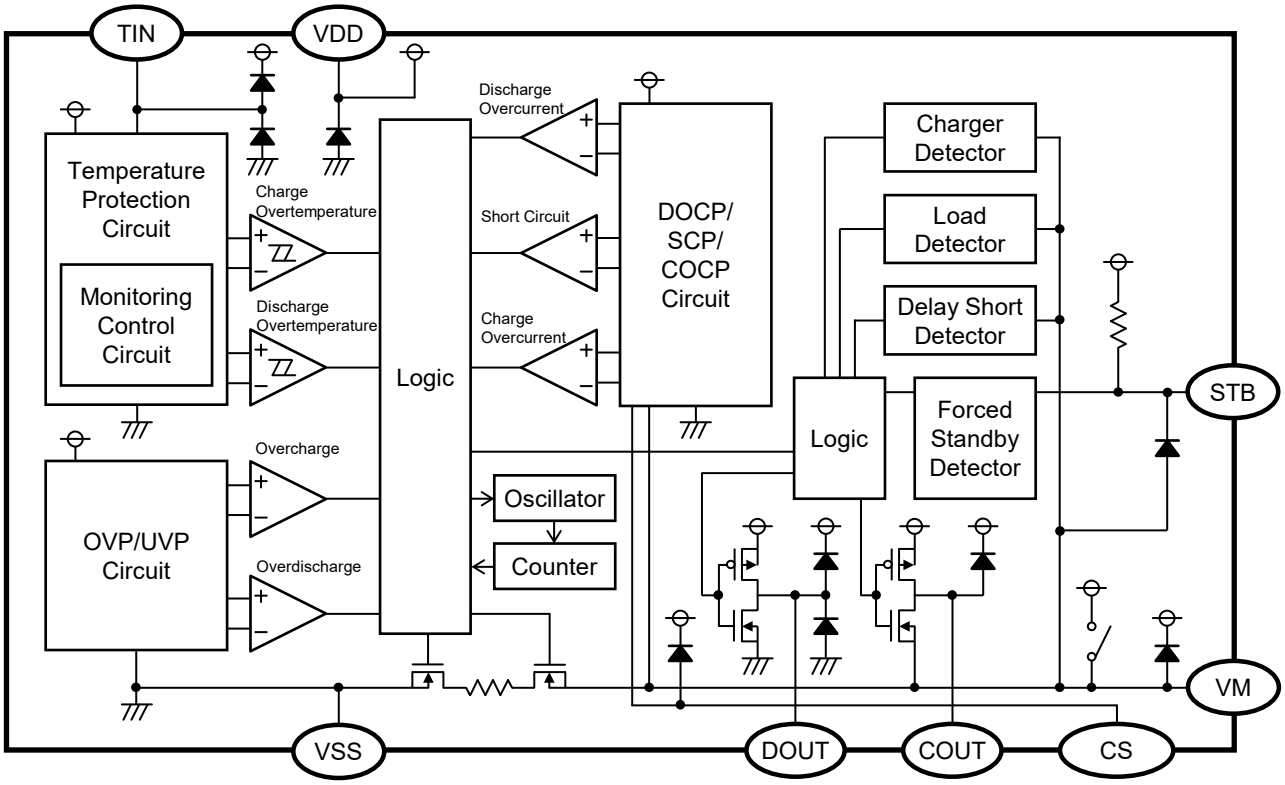
ORDER INFORMATION

Product Name	Package	RoHS	Halogen-Free	Plating Composition	Weight [mg]	MOQ [pcs]
NB7130ZA *****E2S	WLCSP-8-ZA1	Yes	Yes	TBD	TBD	5,000

BLOCK DIAGRAM

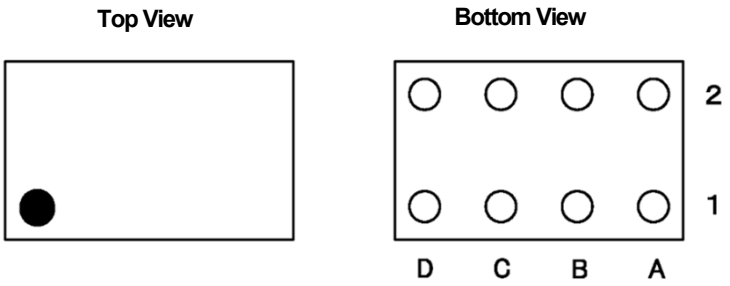


NB7130ZA (STB Pin Active-high) Block Diagram



NB7130ZA (STB Pin Active-low) Block Diagram

PIN DESCRIPTIONS



NB7130ZA (WLCSP-8-ZA1) Pin Configuration

Pin No.	Pin Name	I/O	Description
A1	VM	I	Battery pack minus voltage input pin
B1	VDD	I	Power supply pin, the substrate level of the IC
C1	STB	I	Forced standby control input pin
D1	VSS	-	Ground pin for the IC
A2	COUT	O	Charge control pin, CMOS output
B2	CS	I	Current sensing input pin
C2	TIN	I	Temperature sensing input pin
D2	DOUT	O	Discharge control pin, CMOS output

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	–0.3 to 12	V
VM Pin Input Voltage	V_{VM}	V_{DD} – 30 to V_{DD} + 0.3	V
CS Pin Input Voltage	V_{CS}	V_{DD} – 30 to V_{DD} + 0.3	V
TIN Pin Input Voltage	V_{TIN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
STB Pin Input Voltage	V_{STB}	V_{VM} – 0.3 to V_{DD} + 0.3	V
COUT Pin Output Voltage	V_{COUT}	V_{DD} – 30 to V_{DD} + 0.3	V
DOUT Pin Output Voltage	V_{DOUT}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D	150	mW
Junction Temperature Range	Tj	–40 to 125	°C
Storage Temperature Range	Tstg	–55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION VOLTAGE

	Symbol	Rating	Unit
HBM (Human Body Model)	C = 100 pF, R = 1.5 kΩ	±2000	V
CDM (Charged Device Model)	Field Included CDM (FI-CDM)	±1000	V

ELECTROSTATIC DISCHARGE RATINGS

The electrostatic discharge test is done based on JEDEC JS001, JS002.

RECOMMENDED OPERATING CONDITIONS

	Symbol	Rating	Unit
Operating Input Voltage	V_{OPE}	1.5 to 5.0	V
Operating Temperature Range	Ta	–40 to 105 (TBD)	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

Voltages are defined as $V_{DD} - V_{SS}$, Ta = 25°C, unless otherwise specified in Conditions.

NB7130ZA Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Minimum Charging Voltage for 0 V Battery Charger	V_{STCHG}	Defined as $V_{DD} - V_{VM}$, V_{DD} = 0 V	-	-	1.8	V
0 V Battery Charging Inhibition Voltage	V_{NOCHG}	R_{VDD} = 330Ω, $V_{VM} = V_{CS}$ = –0.6 V	V_{NOCHG} – 0.020	V_{NOCHG}	V_{NOCHG} + 0.020	V
0 V Battery Charging Inhibition Detection Delay Time	$t_{VNOCHGDET}$	$V_{DD} = V_{DET2} - 0.1$ V → $V_{NOCHG} - 0.1$ V, $V_{VM} = V_{CS}$ = –0.6 V	-	-	300 (TBD)	µs
0 V Battery Charging Inhibition Release Delay Time	$t_{VNOCHGREL}$	$V_{DD} = V_{NOCHG} - 0.1$ V → $V_{DET2} - 0.1$ V, $V_{VM} = V_{CS}$ = –0.6 V	-	-	300 (TBD)	µs
Overcharge Detection Voltage	V_{DET1}	R_{VDD} = 330Ω	V_{DET1} – 0.0065	V_{DET1}	V_{DET1} + 0.0065	V
Overcharge Release Voltage	V_{REL1}	R_{VDD} = 330Ω, $V_{VM} = V_{CS}$ = 1.0 V	V_{DET1} – 0.0115	V_{DET1}	V_{DET1} + 0.0065	V
Overcharge Detection Delay Time	t_{VDET1}	V_{DD} = 3.9 V → V_{DET1} + 0.1 V, $V_{VM} = V_{CS}$ = 0 V	t_{VDET1} × 0.80	t_{VDET1}	t_{VDET1} × 1.20	ms
Overcharge Release Delay Time	t_{VREL1}	$V_{DD} = V_{DET1}$ + 0.1 V → 3.9 V, $V_{VM} = V_{CS}$ = 1.0 V	1.65	2.1	2.55	ms
Over-discharge Detection Voltage	V_{DET2}	V_{VM} = 0 V, R_{VDD} = 330Ω	V_{DET2} – 0.0170	V_{DET2}	V_{DET2} + 0.0170	V
Over-discharge Release Voltage	V_{REL2}	V_{VM} = 0 V, R_{VDD} = 330Ω				
		Over-discharge: Latch	V_{DET2} – 0.0170	V_{DET2} + 0.008	V_{DET2} + 0.0320	V
		Over-discharge: Latch with Hysteresis	V_{REL2} – 0.0700	V_{REL2}	V_{REL2} + 0.0700	V
Over-discharge Detection Delay Time	t_{VDET2}	V_{DD} = 3.9 V → V_{DET2} – 0.1 V, V_{VM} = 0 V	t_{VDET2} × 0.80	t_{VDET2}	t_{VDET2} × 1.20	ms
Over-discharge Release Delay Time	t_{VREL2}	$V_{DD} = V_{DET2} - 0.1$ V → 3.9 V, V_{VM} = 0 V	0.85	1.10	1.35	ms
Discharge Overcurrent Detection Voltage	V_{DET3}	Defined as $V_{VM} - V_{CS}$, V_{DD} = 3.9 V	V_{DET3} – 0.00075	V_{DET3}	V_{DET3} + 0.00075	V
Discharge Overcurrent Release Voltage	V_{REL3}	Defined as $V_{VM} - V_{SS}$, V_{DD} = 3.9 V,				
		V_{REL3} = 0 V	– 0.02	0.00	0.02	V
		V_{REL3} = 0.04 V	0.015	0.04	0.065	V
		V_{REL3} = 0.2 V	0.05	0.20	0.35	V
		$V_{REL3} = V_{DD} \times 0.130$ V	V_{DD} × 0.115	V_{DD} × 0.130	V_{DD} × 0.150	V
Discharge Overcurrent Detection Delay Time	t_{VDET3}	V_{DD} = 3.9 V, $V_{VM} - V_{CS}$ = 0 V → V_{DET3} + 0.01 V	t_{VDET3} × 0.80	t_{VDET3}	t_{VDET3} × 1.20	ms
Discharge Overcurrent Release Delay Time	t_{VREL3}	V_{DD} = 3.9 V, $V_{CS} = V_{VM}$ = 1.0 V → –0.1 V	0.85	1.10	1.35	ms
Short Circuit Detection Voltage 1	V_{SHORT1}	Defined as $V_{VM} - V_{CS}$, V_{DD} = 3.9 V,				
		$V_{SHORT1} \leq$ 0.080 V	V_{SHORT1} – 0.0010	V_{SHORT1}	V_{SHORT1} + 0.0010	V
		$V_{SHORT1} \leq$ 0.125 V	V_{SHORT1} – 0.0020	V_{SHORT1}	V_{SHORT1} + 0.0020	V
Short Circuit Detection Voltage 2	V_{SHORT2}	Defined as $V_{VM} - V_{SS}$, V_{DD} = 3.9 V	V_{DD} – 2.00	V_{DD} – 1.50	V_{DD} – 0.80	V

NB7130ZA Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Short Circuit Detection Delay Time 1	$t_{VSHORT1}$	V_{DD} = 3.9 V, V_{CS} = 0 V, V_{VM} = 0V → V_{SHORT1} + 0.01 V,				
		$t_{VSHORT1}$ = 0.28 ms	0.210	0.280	0.350	ms
		$t_{VSHORT1}$ = 0.53 ms	0.397	0.530	0.663	ms
		$t_{VSHORT1}$ = 1.10 ms	0.85	1.10	1.35	ms
		$t_{VSHORT1}$ = 2.10 ms	1.65	2.10	2.55	ms
Short Circuit Detection Delay Time 2	$t_{VSHORT2}$	V_{DD} = 3.9 V, V_{CS} = V_{VM} = 0 V → 3.9 V	0.85	1.1	1.35	ms
Charge Overcurrent Detection Voltage	V_{DET4}	Defined as V_{VM} – V_{CS}, V_{DD} = 3.9 V	V_{DET4} – 0.00075	V_{DET4}	V_{DET4} + 0.00075	V
Charge Overcurrent Release Voltage	V_{REL4}	Defined as V_{VM} – V_{SS}, V_{DD} = 3.9 V	–0.02	0.00	0.02	V
Charge Overcurrent Detection Delay Time	t_{VDET4}	V_{DD} = 3.9 V, V_{VM} – V_{CS} = 0 V → –0.1 V	t_{VDET4} × 0.80	t_{VDET4}	t_{VDET4} × 1.20	ms
Charge Overcurrent Release Delay Time	t_{VREL4}	V_{DD} = 3.9 V, V_{CS} = V_{VM} = –1.0 V → 0.1 V	0.85	1.10	1.35	ms
Load Detection Voltage when Overcharging	V_{LDDET1}	Defined as V_{VM} – V_{SS}, V_{DD} = 3.9 V	–0.020	0.000	0.020	V
Load Detection Voltage when Over-discharging	V_{LDDET2}	Defined as V_{VM} – V_{SS}, V_{DD} = 1.9 V	V_{DD} – 1.50	V_{DD} – 1.00	V_{DD} – 0.50	V
Load Detection Voltage when Over-discharging Detection Delay Time	$t_{VLDDET2}$	V_{VM} - V_{SS} = 0 V → V_{LDDET2} + 0.1V	-	-	300 (TBD)	µs
Charger Detection Voltage	V_{CHGDET}	Defined as V_{VM} – V_{SS}, R_{VM} = 1kΩ,				
		V_{DD} = 1.9 V	0.2 (TBD)	0.6 (TBD)	1.0 (TBD)	V
		V_{DD} = 3.9 V	0.4	0.7	1.0	V
Charger Detection Delay Time	$t_{VCHGDET}$	V_{VM} - V_{SS} = V_{DD} → V_{CHGDET} - 0.1V	-	-	300 (TBD)	µs
COUT Pin Output Low Voltage	V_{COL}	I_{COUT} = 50µA, V_{DD} = 4.85 V	-	0.4	0.5	V
COUT Pin Output High Voltage	V_{COH}	I_{COUT} = –50µA, V_{DD} = 3.9 V	3.4	3.7	-	V
DOUT Pin Output Low Voltage	V_{DOL}	I_{DOUT} = 50µA, V_{DD} = 1.9 V	-	0.2	0.5	V
DOUT Pin Output High Voltage	V_{DOH}	I_{DOUT} = –50µA, V_{DD} = 3.9 V	3.4	3.7	-	V
VM Pin Output Pullup Resistance	R_{VMPU}	Pulled up to V_{DD}	100 (TBD)	300 (TBD)	500 (TBD)	kΩ
VM Pin Output Pulldown Resistance	R_{VMPD}	Pulled down to V_{SS}	20 (TBD)	45 (TBD)	70 (TBD)	kΩ
Supply Current	I_{DD}	V_{DD} = 3.9 V, V_{VM} = 0 V	-	3.0	6.0	µA
Temperature Sensing Input Current	I_{TIN}	V_{DD} = 3.9 V, V_{VM} = 0 V,				
		NTC Resistance = 470 kΩ, t_{TOFF} = 128ms	-	-	0.50	µA
		NTC Resistance = 100 kΩ, t_{TOFF} = 128ms	-	-	2.00	µA
		NTC Resistance = 470 kΩ, t_{TOFF} = 512ms	-	-	0.15	µA
		NTC Resistance = 100 kΩ, t_{TOFF} = 512ms	-	-	0.50	µA
Standby Current	$I_{STANDBY}$	V_{DD} = 1.9 V	-	-	0.04	µA

NB7130ZA Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Charge Overtemperature Detection Temperature	T_{DET1}	V_{DD} = 3.9 V, [NTC performance] Vender: muRata Part: NCP02WF474F05RH Resistance: 470kΩ±1%(25°C) Part: NCP03WF104F05RL Resistance: 100kkΩ±1%(25°C) B-Constant: 4250K±1%	T_{DET1} – 2.0	T_{DET1}	T_{DET1} + 2.0	°C
Charge Overtemperature Release Temperature	T_{REL1}		T_{REL1} – 3.0	T_{REL1}	T_{REL1} + 3.0	°C
Discharge Overtemperature Detection Temperature	T_{DET2}		T_{DET2} – 2.0	T_{DET2}	T_{DET2} + 2.0	°C
Discharge Overtemperature Release Temperature	T_{REL2}		T_{REL2} – 3.0	T_{REL2}	T_{REL2} + 3.0	°C
Temperature Detection Delay Time	t_{TDET}	V_{DD} = 3.9 V	t_{TDET} × 0.80	t_{TDET}	t_{TDET} × 1.20	ms
Temperature Release Delay Time	t_{TREL}	V_{DD} = 3.9 V	102	128	154	ms
Temperature Sensing Intermittent ON Time	t_{TON}	V_{DD} = 3.9 V	6.4	8	9.6	ms
Temperature Sensing Intermittent OFF Time	t_{TOFF}	V_{DD} = 3.9 V	t_{TOFF} × 0.80	t_{TOFF}	t_{TOFF} × 1.20	ms
TIN Pin Internal Resistance	R_{TIN}	Pulled down to V_{SS}, NTC Resistance = 470 kΩ NTC Resistance = 100 kΩ	 90 (TBD) 19 (TBD)	 150 (TBD) 33 (TBD)	 210 (TBD) 47 (TBD)	 kΩ kΩ
Forced Standby Detection Voltage	V_{STBDET}	Defined as V_{STB} – V_M, V_{DD} = 3.9 V	0.7 (TBD)	1.2 (TBD)	1.7 (TBD)	V
Forced Standby Release Voltage	V_{STBREL}	Defined as V_{VM} – V_{SS}, V_{DD} = 3.9 V	Same V_{REL3} or V_{REL4}			V
Forced Standby Detection Delay Time	$t_{VSTBDET}$	V_{DD} = 3.9 V, V_{STB} – V_M = 0V → 3.9 V, when Active-high when Active-low	 $t_{VSTBDET}$ × 0.80 $t_{VSTBDET}$ × 0.80	 $t_{VSTBDET}$ $t_{VSTBDET}$	 $t_{VSTBDET}$ × 1.20 $t_{VSTBDET}$ × 1.20	 ms ms
Forced Standby Release Delay Time	$t_{VSTBREL}$	V_{DD} = 3.9 V, V_{VM} = 1 V → V_{STBREL} – 0.1 V, $t_{VSTBREL}$ = 1.1 ms $t_{VSTBREL}$ = 16 ms	 0.85 $t_{VSTBREL}$ × 0.80	 1.10 $t_{VSTBREL}$	 1.35 $t_{VSTBREL}$ × 1.20	 ms ms
STB Pin Internal Resistance	R_{STB}	Pulled up to V_{VM}, when Active-high when Active-low	 50 (TBD) 50 (TBD)	 100 (TBD) 100 (TBD)	 170 (TBD) 170 (TBD)	 kΩ kΩ

All test parameters listed in Electrical Characteristics are done under Ta = 25°C only.

● Test Circuits (TBD)

THEORY OF OPERATION (TBD)

● Overcharge Protection

When the VDD pin voltage (V_{DD}) exceeds the overcharge detection voltage (V_{DET1}) for longer than the overcharge detection delay time (t_{VDET1}), the IC enters the overcharge protection state. In this state, the COUT pin outputs Low, turning off the charge-control FET and stopping charging.
Even while the charge-control FET is OFF, discharge current can flow through the parasitic body diode of the FET. When this occurs, the VM pin voltage (V_{VM}) is higher than the VSS pin voltage (V_{SS}) by approximately the diode's forward voltage (V_F).
To release from the overcharge protection state, the following conditions must be satisfied.

Type	Pin Conditions	Delay Time	Remarks
Latch	$V_{VM} > V_{LDDET1}$ and $V_{DD} < V_{REL1}$	t_{VREL1}	-

● Over-discharge Protection

When the VDD pin voltage (V_{DD}) falls below the over-discharge detection voltage (V_{DET2}) for longer than the over-discharge detection delay time (t_{VDET2}), the IC enters the over-discharge protection state. In this state, the DOUT pin outputs Low, turning OFF the discharge-control FET and stopping discharging.
Even while the discharge-control FET is OFF, charge current can flow through the parasitic body diode of the FET. When this occurs, the VM pin voltage (V_{VM}) is lower than the VSS pin voltage (V_{SS}) by approximately the diode's forward voltage (V_F).
After the discharge-control FET is turned OFF, once V_{VM} exceeds the load detection voltage (V_{LDDET2}), the IC moves to the standby state, minimizing the current consumption.
To release from the over-discharge protection state, the following conditions must be satisfied.

Type	Pin Conditions	Delay Time	Remarks
Latch	$V_{VM} < V_{CHGDET1}$ and $V_{DD} > V_{REL2}$	t_{VREL2}	V_{VM} is pulled up to the V_{DD} internally.

● Discharge Overcurrent Protection

The IC monitors the discharge current via the sense voltage V_{SENS}—the voltage between the CS and VM pins that appears across the sense resistor (R_{SENS}).
When V_{SENS} exceeds $V_{DET3}$for longer than the discharge-overcurrent detection delay time (t_{VDET3}), the IC enters the discharge overcurrent protection state. In this state, the DOUT pin outputs Low, turning OFF the discharge-control FET and stopping the discharge overcurrent.
To release from the discharge overcurrent protection state, the following conditions must be satisfied.

Type	Pin Condition	Delay Time	Remarks
Auto Release	$V_{VM} < V_{REL3}$	t_{VREL3}	V_{VM} is pulled down to the V_{SS} internally. Note1 (R_{VMPD} = Typ.45kΩ)
Latch	$V_{VM} < V_{REL3}$	t_{VREL3}	V_{VM} is pulled up to the V_{DD} internally.

Note1: In the discharge-overcurrent state, V_{VM} is calculated by the following equation.

$$V_{VM} = V_{CELL} \times R_{VMPD} / (R_{VMPD} + R_{VM} + R_{LOAD})$$

V_{CELL} : Battery voltage
R_{VMPD} : VM pin pulled down resistance
R_{VM} : External resistance for VM pin
R_{LOAD} : Load resistance to a battery pack

● Short-circuit Protection

The IC monitors the discharge current via the sense voltage V_{SENS}—the voltage between the CS and VM pins that appears across the sense resistor (R_{SENS}).
When V_{SENS} exceeds the short-circuit detection voltage (V_{SHORT1}) for longer than the short-circuit detection delay time (t_{VSHORT}), the IC enters the short-circuit protection state. In this state, the DOUT pin outputs Low, turning OFF the discharge-control FET and stopping the short-circuit current.
To release from the short-circuit protection state, the same conditions and timing used for *Discharge Overcurrent Protection* apply.

● Charge Overcurrent Protection

The IC monitors the charge current via the sense voltage V_{SENS}—the voltage between the CS and VM pins that appears across the sense resistor (R_{SENS}).
When V_{SENS} falls below the charge-overcurrent detection voltage (V_{DET4}) for longer than the charge-overcurrent detection delay time (t_{VDET4}), the IC enters the charge overcurrent protection state. In this state, the COUT pin outputs Low, turning OFF the charge-control FET and stopping the charge overcurrent.
To release from the charge overcurrent protection state, the following condition must be satisfied.

Type	Pin Condition	Delay Time	Remarks
Auto Release	$V_{VM} > V_{REL4}$	t_{VREL4}	V_{VM} is pulled up to the V_{DD} internally.

● 0 V Battery Charging

The IC includes a selectable function that determines whether a battery discharged to 0 V may be charged.

0 V Battery Charge Function "Permission"

0 V Battery Charging is allowed. The charge-control FET turns ON and the battery can recover from 0 V.

0 V Battery Charge Function "Inhibition"

When the VDD pin voltage (V_{DD}) falls below the 0 V battery charging inhibition voltage (V_{NOCHG}) and charger is connected, the IC enters the 0 V battery charging inhibition state. In this state, the COUT pin outputs Low, turning OFF the charge-control FET and stopping 0 V battery charging.

● Forced Standby Function

The IC includes an optional forced standby function assigned to the STB pin. When the forced standby function is enabled, the IC operates as follows:

When the STB pin voltage (V_{STB}) exceeds the forced standby detection voltage (V_{STBDET}) for longer than the forced standby detection delay time (t_{STBDET}), the IC enters the pre-forced standby state. In this state, the DOUT pin outputs Low, turning OFF the discharge-control FET and stopping discharging.

Even while the discharge-control FET is OFF, charge current can flow through the parasitic body diode of the FET. When this occurs, the VM pin voltage (V_{VM}) is lower than the VSS pin voltage (V_{SS}) by approximately the diode's forward voltage (V_F).

After the discharge-control FET is turned OFF, once V_{VM} exceeds the load detection voltage (V_{LDDET2}), the IC moves to the forced standby state, minimizing the current consumption.

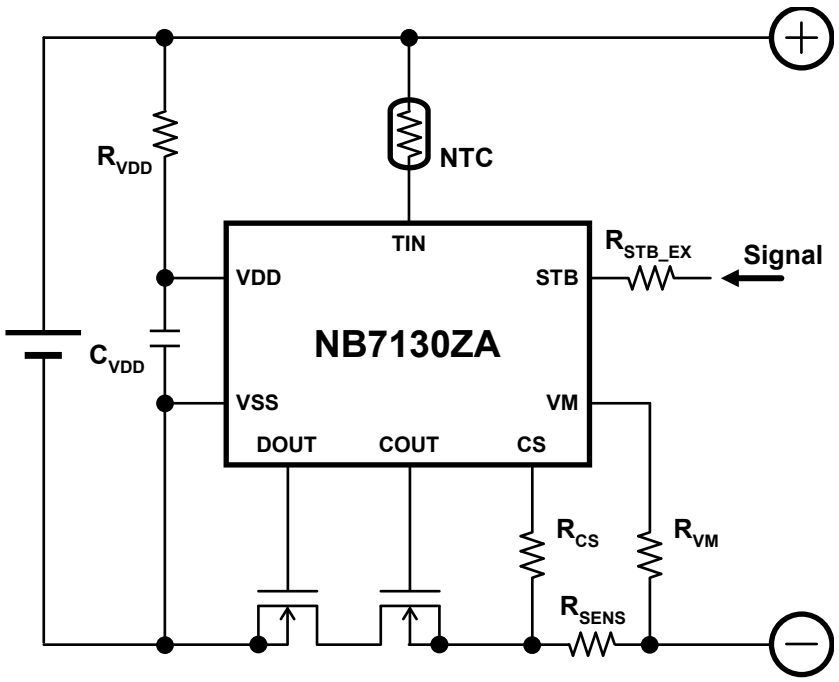
To release from the forced standby state, the following conditions must be satisfied.

Type	Pin Conditions	Delay Time	Remarks
Latch	$V_{VM} < V_{STBREL}$ (in pre-forced standby state) or $V_{VM} < V_{CHGDET}$ (in forced standby state)	$t_{VSTBREL}$ or $t_{VCHGDET}$	V_{VM} is pulled up to the V_{DD} internally.

● Timing Chart (TBD)

APPLICATION INFORMATION

● Typical Application Circuit (TBD)



NB7130ZA Typical Application Circuit

External Components

Symbol	Min.	Typ.	Max.
Resistor			
R_{VDD}	-	330Ω	1.0kΩ
R_{VM}	330 Ω	1.0kΩ	1.3kΩ
R_{CS}	330 Ω	1.0kΩ	1.3kΩ
R_{STB_EX}	-	1.0kΩ	-
R_{SENS}	-	1.5mΩ	-
Capacitor			
C_{VDD}	0.01μF	0.10μF	1.00μF

The NTC thermistor with the following characteristics is required.

Vendor	muRata	
Part Number	NCP02WF474F05RH	NCP03WF104F05RL
Resistance	470kΩ±1% (25°C)	100kΩ±1% (25°C)
B-Constant	4250K ±1%	4250K ±1%

The voltage flucuation is stabilized by R_{VDD} and C_{VDD}. If R_{VDD} is too large, the detection voltage rises by the conduction current at detection. To stabilize the operation, it is recommended to use a resistor of 330Ω or less for R_{VDD} and a capacitor of 0.01μF to 1.00μF for C_{VDD}.

When the R_{SENS} of the resistor sensing the overcurrent is too large, the power loss also become large. If the R_{SENS} is inappropriate for the overcurrent, the power loss may exceed the allowable loss of the R_{SENS}. The appropriate R_{SENS} should be selected according to the cell specifications.

In addition, when a reverse charger is connected, the external resistors must meet the following requirements to suppress the current flowing from the pack side pin to the VDD pin.

Reverse Charge Current Path	Recommended Resistance Conditions
From CS pin to VDD pin	$R_{VM} = R_{CS} \geq 330\ \Omega$ Note
From VM pin to VDD pin	

Note: If R_{VM} is larger than the requirement, charger connection may not be recognized that is required to release from some abnormal detection states.

This application circuit diagram is an example. The performance of the circuit depends on the PCB layout and external components. In the actual application, fully evaluation is required.

TECHNICAL NOTES

A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

- Please evaluate the product at the PCB level before use, as some symptoms may remain that cannot be confirmed by the evaluation at the IC level.
- When using any coating or underfill to improve moisture resistance or joining strength, evaluate them adequately before using. In certain materials or coating conditions, corrosion by contained constituents, current leakage by moisture absorption, crack and delamination by physical stress can happen. If the curing temperature of the coating material or underfill material exceeds the absolute maximum rating, the electrical characteristics of this product may change.
- When performing X-ray inspection in mass production process and evaluation build stage such as the product functions and characteristics confirmation, please confirm X-ray irradiation does not exceed 1.5Gy (absorbed dose for air).

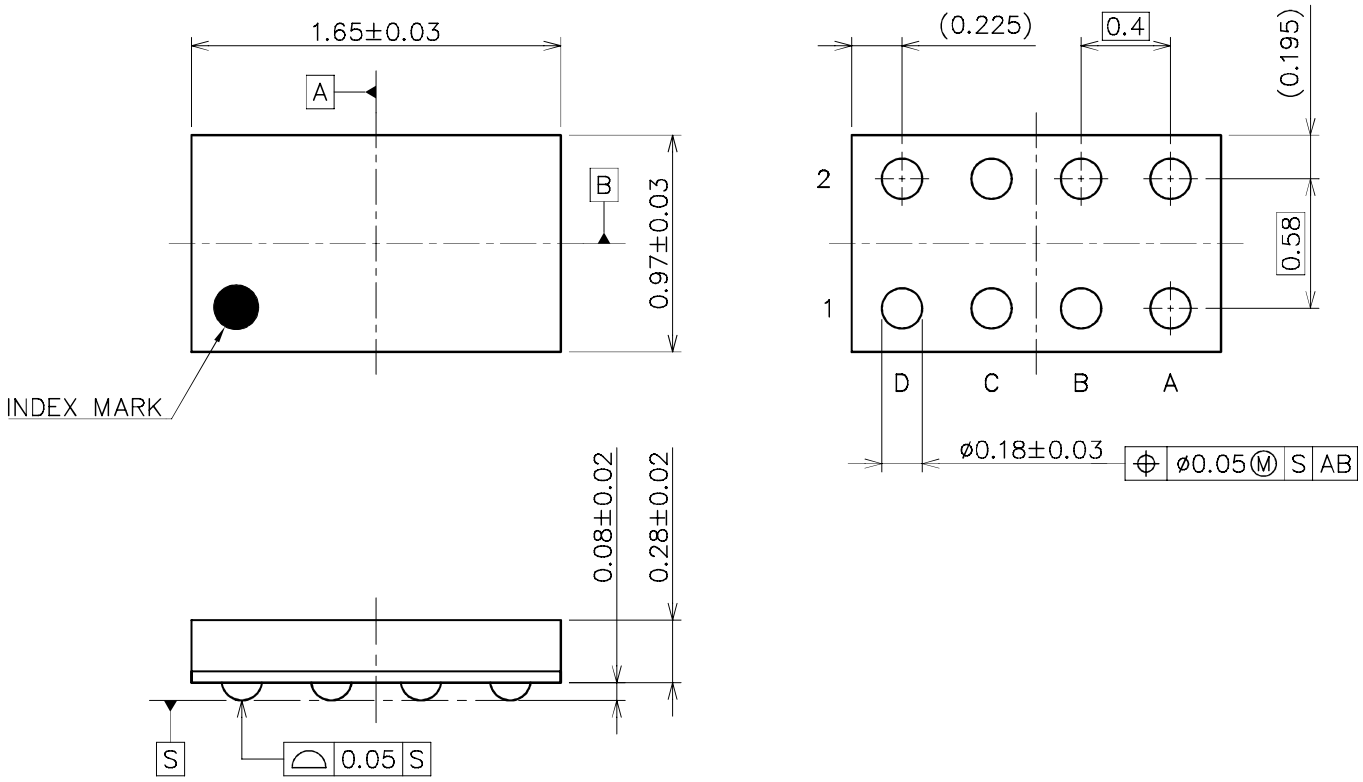
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PI-WLCSP-8-ZA1-E-B

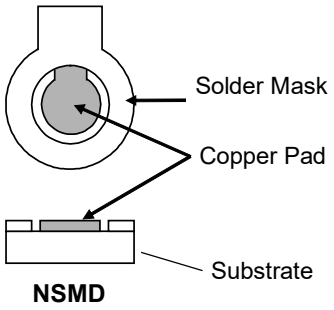
■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS

Recommended Land Pattern



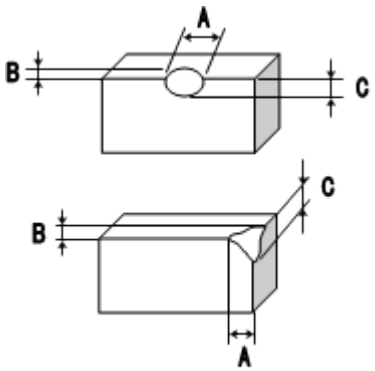
NSMD Pad Definition		
Pad definition	Copper Pad	Solder Mask Opening
NSMD (Non-Solder Mask defined)	0.18mm	MIN. 0.28mm

*) Pad Layout and size can modify by customers material, equipment and method.
*) Please adjust pad layout according to your conditions.
*) Recommended Stencil Aperture Size: ϕ0.26mm

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■ Visual Inspection Criteria

No.	Inspection Items	Inspection Criteria	Figures
1	Package chipping	A ≥ 0.2mm is rejected B ≥ 0.2mm is rejected C ≥ 0.2mm is rejected And, Package chipping to Si surface and to bump is rejected.	
2	Si surface chipping	A≥0.2mm is rejected B≥0.2mm is rejected C≥0.2mm is rejected But, even if A ≥ 0.2mm, B ≤ 0.1mm is acceptable.	
3	No bump	No bump is rejected.	
4	Marking miss	To reject incorrect marking, such as another product name marking or another lot No. marking.	
5	No marking	To reject no marking on the package.	
6	Reverse direction of marking	To reject reverse direction of marking character.	
7	Defective marking	To reject unreadable marking. (Microscope: X15/ White LED/ Viewed from vertical direction)	
8	Scratch	To reject unreadable marking character by scratch. (Microscope: X15/ White LED/ Viewed from vertical direction)	
9	Stain and Foreign material	To reject unreadable marking character by stain and foreign material. (Microscope: X15/ White LED/ Viewed from vertical direction)	

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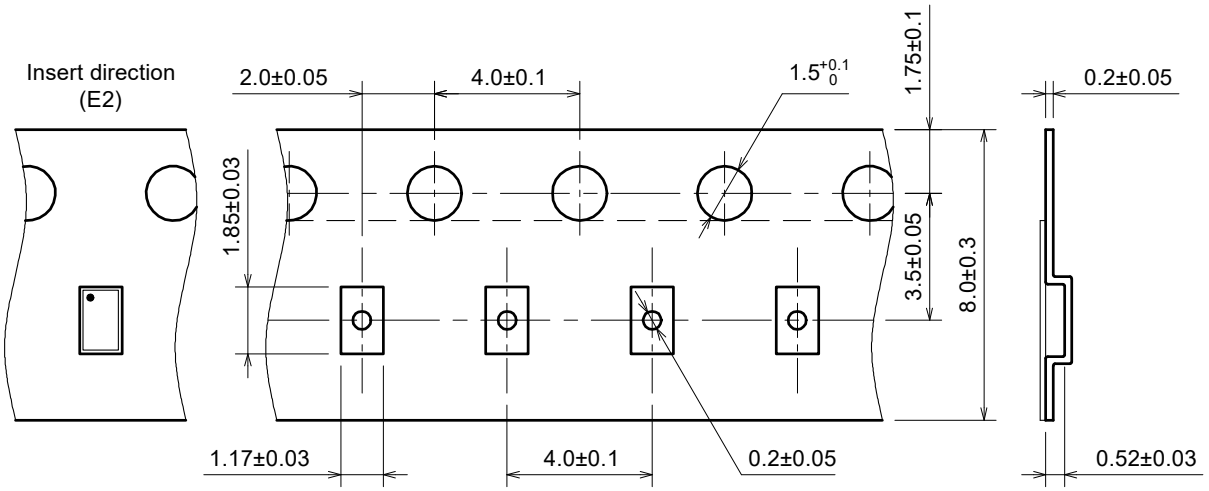
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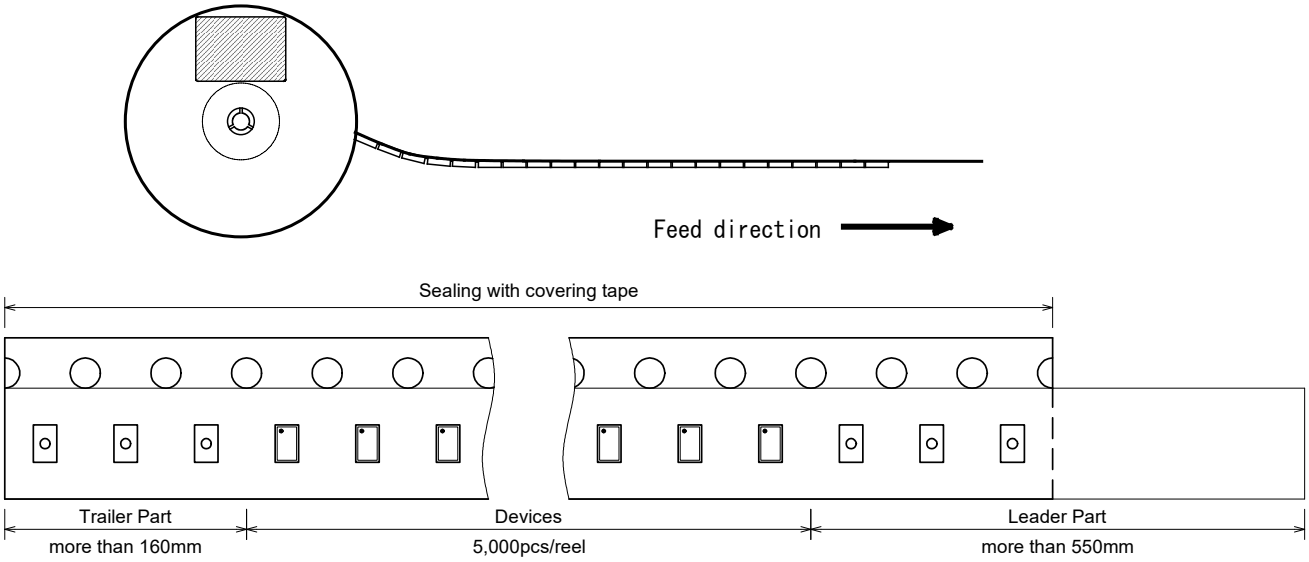
■ PACKING SPEC

UNIT: mm

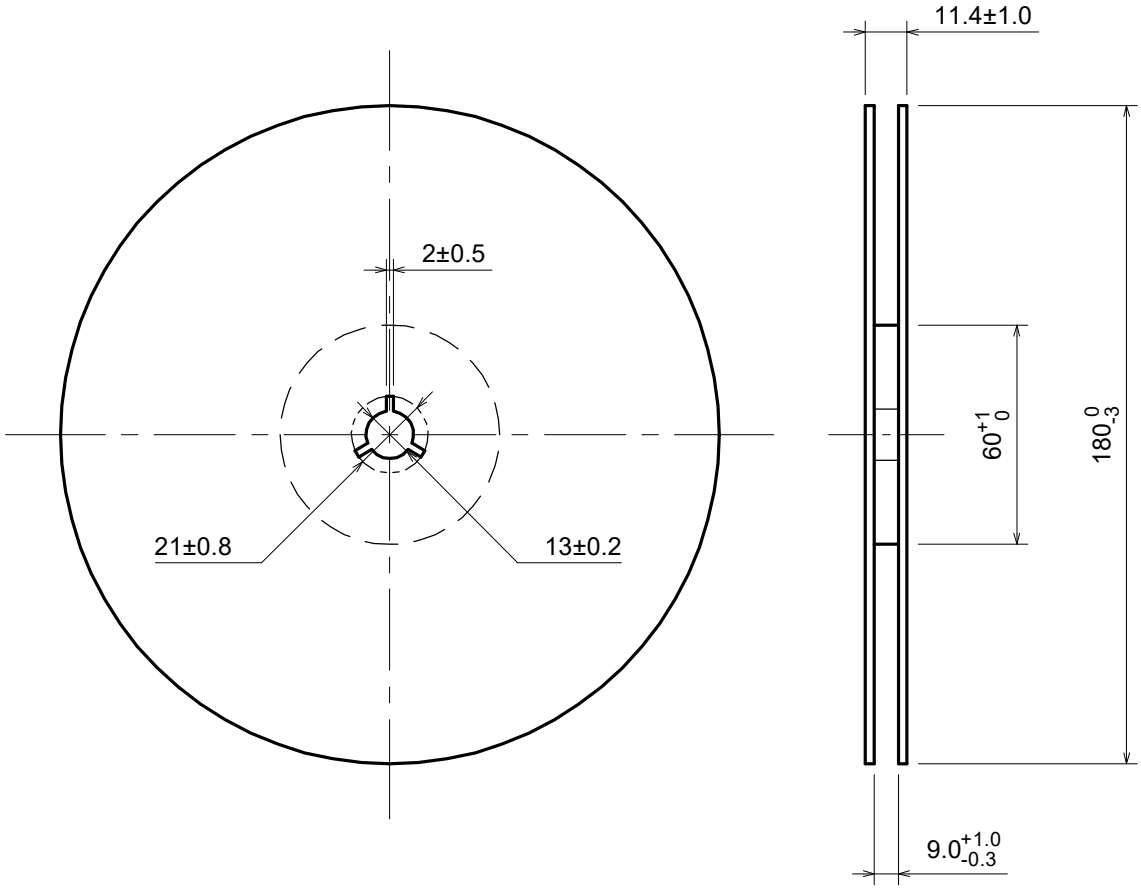
(1) Taping dimensions / Insert direction



(2) Taping state



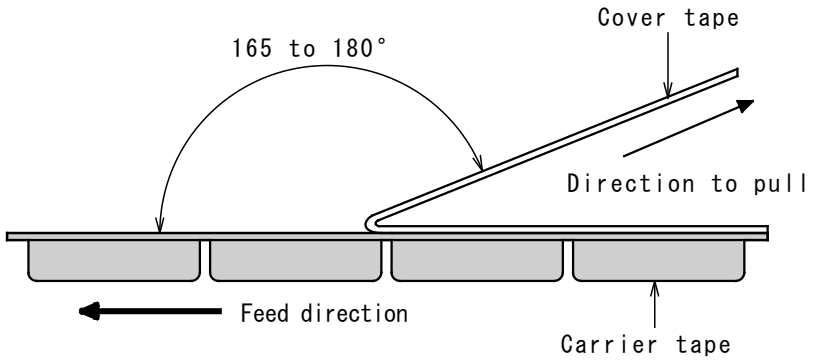
(3) Reel dimensions



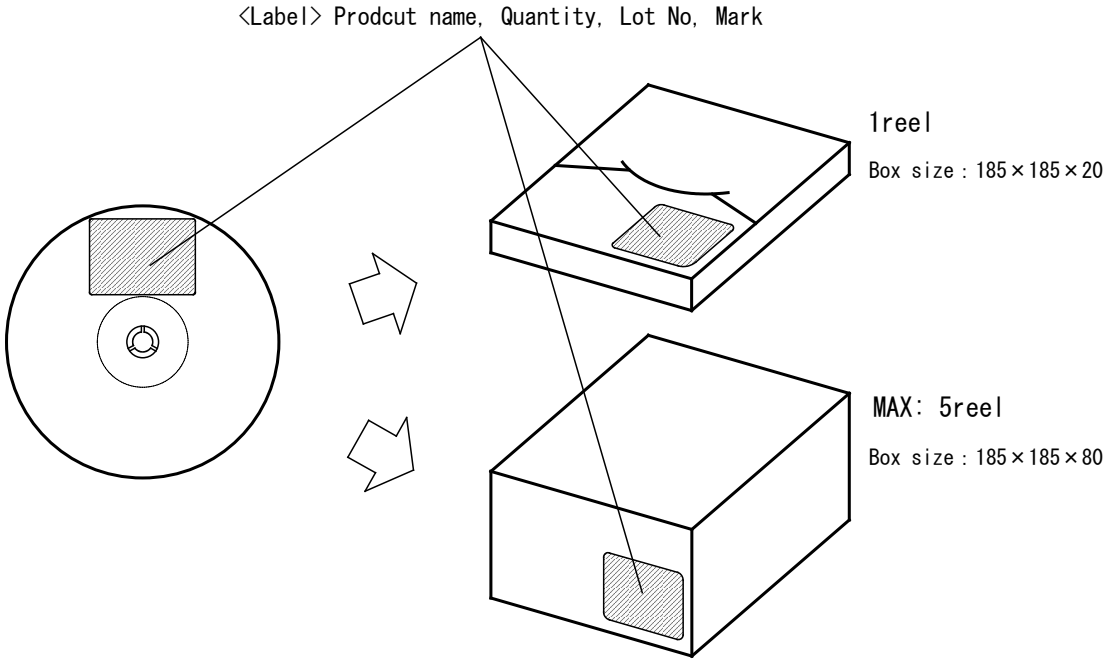
(4) Peeling strength

Peeling strength of cover tape

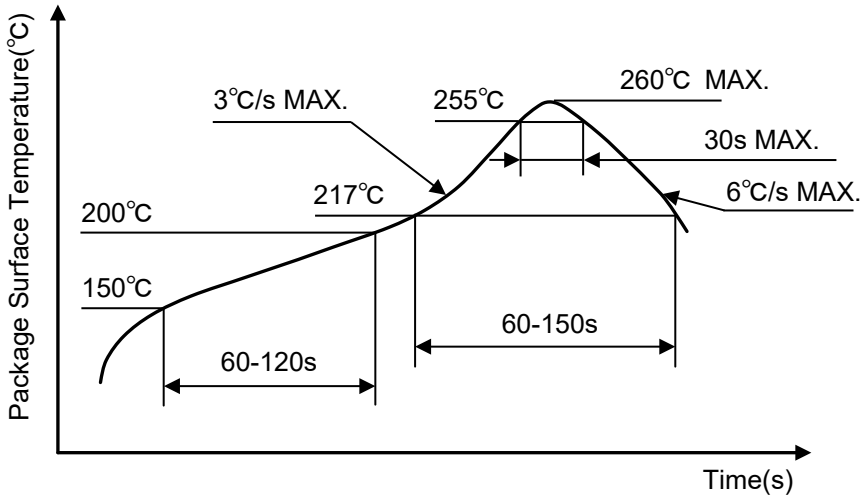
・Peeling angle	165 to 180° degrees to the taped surface.
・Peeling speed	300mm/min
・Peeling strength	0.1 to 1.0N



(5) Packing state



■ **HEAT-RESISTANCE PROFILES**



Reflow profile

PRELIMINARY SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

REVISION HISTORY

Date	Version		Changes
Preliminary Version			
May 30, 2025	0.10	-	Preliminary datasheet release
June 16, 2025	0.20	a	Updated the typical application circuit to add an external resistor of R_{STB_EX}. Added Package Information.

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    - Life Maintenance Medical Equipment
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    - Various Safety Devices
    - Traffic control system
    - Combustion equipment

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    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
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    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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