Product Brief

MEP100

100G ST 2110 SmartNIC Solution

Optimizing Solutions with ST 2110 SmartNIC

A SMPTE ST 2110 - aware SmartNIC is a COTS add-in card providing access to an accelerated media protocol stack implemented in a built-in FPGA. Using the accelerated network stack, a broadcast application can send and receive full frame video, audio and ancillary data to and from the card.

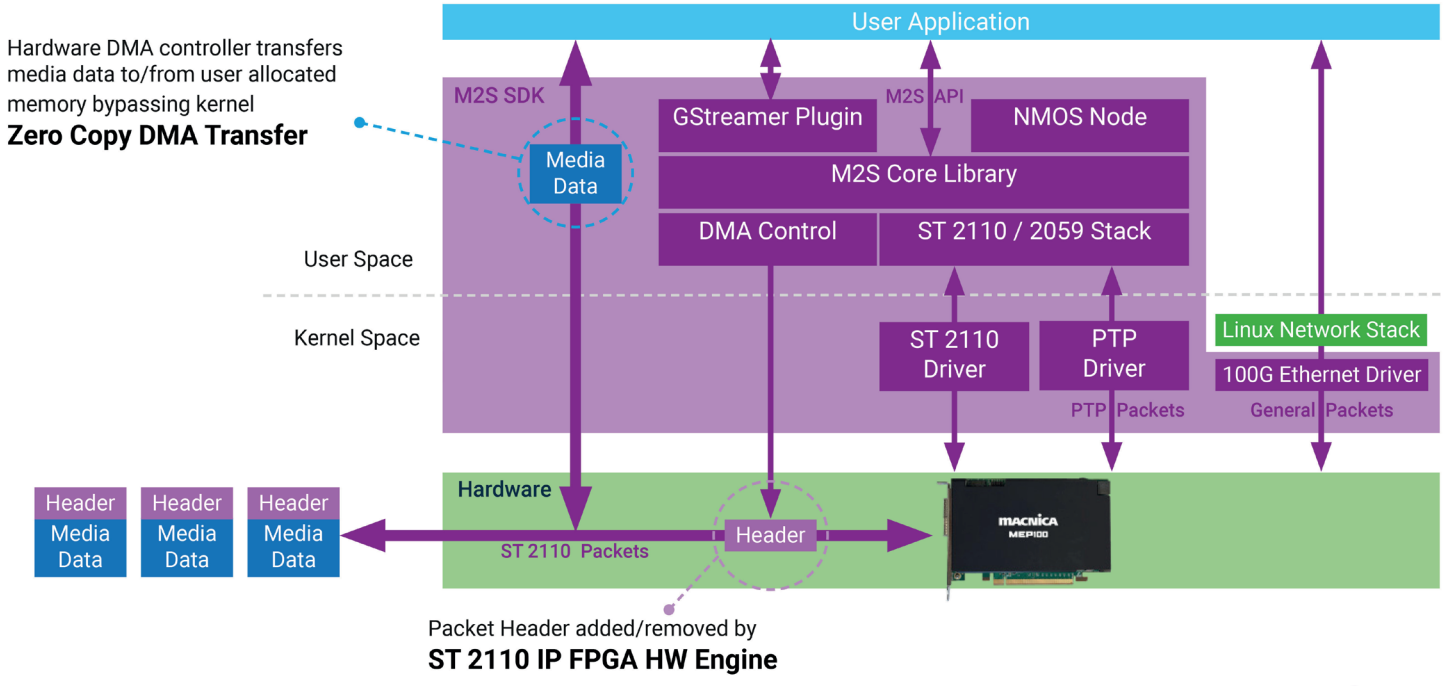
Using the MEP100 ST 2110 SmartNICs, software-based applications can easily process ST 2110 flows without compromizing system resources or network integrity - all the while providing deterministic, scalable, and repeatable ST 2110 environments.

Macnica has developed a hardware-accelerated alternative to today's mainly software-based SMPTE ST 2110 100Gb solutions.

The combination of the full hardware implementation of the SMPTE ST 2110 protocol stack - including PTP timestamping, packet pacing, and hitless protection switching - and a fully featured mutichannel Direct Memory Access (DMA) engine, allows media content to be transferred directly from and to the host CPU memory and the ST 2110 network card. This is done independent from the CPU with no OS usage.

The Altera FPGA-based NIC cards combined with Macnica's intellectual property cores enable more efficient bandwidth usage over 100Gb networks, providing benefits that includes better power efficiency and lower CPU utilization, while offering OS independent deterministic behavior and overall lower system latency.

High Performance & Balanced Architecture



MACNICA

MEP100

100G ST 2110 SmartNIC Solution

High Performance & Balanced Architecture

- Macnica MEP100 - 100G ST 2110 SmartNIC provides a special and unique ST 2110 stream processing solution
- Accelerations by Macnica ST 2110 hardware engine
  - » ST 2110 packets are processed by hardware with no CPU usage for packet header handling
- Fastest media route by Kernel Bypass Technology
  - » Direct transfer to/from allocated user memory
- Flexibility of Linux Network Stack
  - » General Ethernet packets are handled by reliable Linux network stack

M2S SDK

- Simple and intuitive API for media data
  - » Read & write of Video/Ancillary data by frame or subframe unit
  - » Read & write of Audio data by millisecond unit
  - » No need to handle ST 2110 packet data. Media is in samples and frames, ready to be used by your application
- GStreamer plugin support
  - » Video sink
  - » Audio source
  - » Audio sink
- NMOS node support
  - » IS-04
  - » IS-05

Target Features and Specifications

	Features	Specifications	Notes
Software	Target OS	Linux	
	User Interface	Macnica M2S API	
Ethernet	100GbE x 2		
PCIe Streaming	System Bus	PCIe Gen4 x 16	
	Video Buffer Pixel Format	YUVP : Packed YUV 422 only	U0-Y0-V0-Y1 U2-Y2-V2-Y3
ST 2059	Macnica ST 2059 IP core: FPGA components + SW stack working on host CPU		Offloading to HPS (ARM) is out of scope at this phase
ST 2110-20	Resolution	3840 x 2160p, 1920 x 1080p, 1920 x 1080i	
	Number of Streams	Up to 32 TX and 32 RX	
	Mapping Structure	4:2:2 10 bit	
	Frame Rate (Hz)	59.94, 50	
ST 2110-21	Supported Rate	TX side : Type-N, RX side : Type-W	
ST 2110-22 * (JPEG-XS codec base)	Resolution	3840 x 2160p, 1920 x 1080p, 1920 x 1080i	
	Number of Streams	Up to 4 x TX and 8 x RX	ST 2110-20 and -22 convertible design planned for future release
	Mapping Structure	4:2:2 10 bit	
	Frame Rate (Hz)	59.94, 50	
ST 2110-30	Number of Streams	Up to 32 TX and 32 RX	
	Conformance Level	Level-B + 32 ch	
	Sampling Rate	48 kHz	
	Number of Channels per Stream	1 to 32	Packet time 1ms: up to 8 ch, packet time 125us: up to 32 ch
ST 2110-40 *	Number of Streams	Up to 32 TX and 32 RX	
ST 2022-7	Support Class	Class-A, -B, -C and Class-D	Depending on system memory resource
NMOS	Support Protocol	IS-04 and IS-05	

* Phase 1 Production Release does not support these features

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